



Terawins, Inc.

***Advanced Information
Version 0.2***

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T102 Video Display Controller

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1 Introduction

1.1 Features

■ Cost Effective Highly Integrated Double ADC + ITU656/601 Decoder + 2D Video Decoder + OSD + Scaler + TCON + DAC

- Integrates 9-bit Double Analog to Digital Converters (ADC) & Phase Locked Loop (PLL)
- Scaler supports 2-D adaptive intra-field de-interlacer and non-linear 16:9 aspect ration.
- Requires no external Frame Buffer Memory for deinterlacer.
- ITU656/601 Decoder with digital input ports for standard ITU656/601 input data.
- Advanced On Screen Display (OSD) function
- Programmable Timing Controller (Tcon) for Car TV applications
- Multi-standard color decoder with 2D adaptive comb filter
- Innovative and flexible design to reduce total system cost

Double 9-bit Analog to Digital Converters (ADC)

■ 80MSPS Conversion Rate

- Built-in Pre-amp, mid-level & ground clamp circuit
- Automatic Clamp Control for CVBS, Y and C
- Programmable Static Gain Control or Automatic Gain Control for CVBS or Y/C
- Max Input configuration up to 6xCVBS, 3xS-video

Digital Video Enhancement

■ Chroma Enhancer

- C Supports DCTI, Saturation and Hue adjustment.

Advanced Scaling Engine

■ FIR Based Scaler

- Coefficient based sharpness filters
- Independent vertical and horizontal scaling ratio
- 16:9 Non-linear Aspect ratio

■ LCD Interface

- Provides Gamma correction for panel compensation
- Supports image pan functions

- Programmable Timing Controller
- RGB Triple DAC output

■ Color Management

- RGB Gamma Correction

■ Built-in On Screen Display Engine

- 1K-word OSD SRAM memory
- Supports text or bitmap modes
- Supports character blinking and overlay functions
- Fully programmable character mapping
- Supports alpha blending & Zoom-in/Zoom-out function
- Optional fonts can be stored in off-chip serial EEPROM

■ Crystal Oscillator Circuit

- Direct interface to a (27.0MHz) Crystal
- Also provide a buffered clock output for external Micro-controller

■ Digital Test Pattern Generator

- Programmable standard & special panel burn-in test patterns
- Support special border frame blocking mode

■ Independent Display Phase Lock Loop

- Generates pixel clock output to panel
- Supports free run OSD mode

■ Serial Bus Interface

- Supports 2-wire (normal speed) or 4-wire (high speed) modes

■ Pulse Width Modulation Outputs

■ General Purpose Input Output (GPIO)

■ Design For Testability

- Scan chain insertion
- Separated analog & digital test modes

■ Power Supply: +2.5V & +3.3V

■ Package: 100-pin LQFP

1.2 General Description

The T102 is a highly integrated All-in-one Visual Processor that provides major cost saving solution for the portable applications. T102 has built-in Double high performance ADCs, TCON, Triple DACs, Scaling Machine with sophisticated upscaling and downscaling algorithms. The Innovative

integrated "Frame-Buffer-Less" De-interlacer can significantly reduce system cost. The T102 also integrates On Screen Display engine with 1K-word of SRAM. The device can interface to an external micro-controller through 2-wire serial bus interface.

1.3 Applications

1. 4-inch to 7-inch portable DVD or in-car TV
2. Progressive CRT TV

1.4 System Architecture

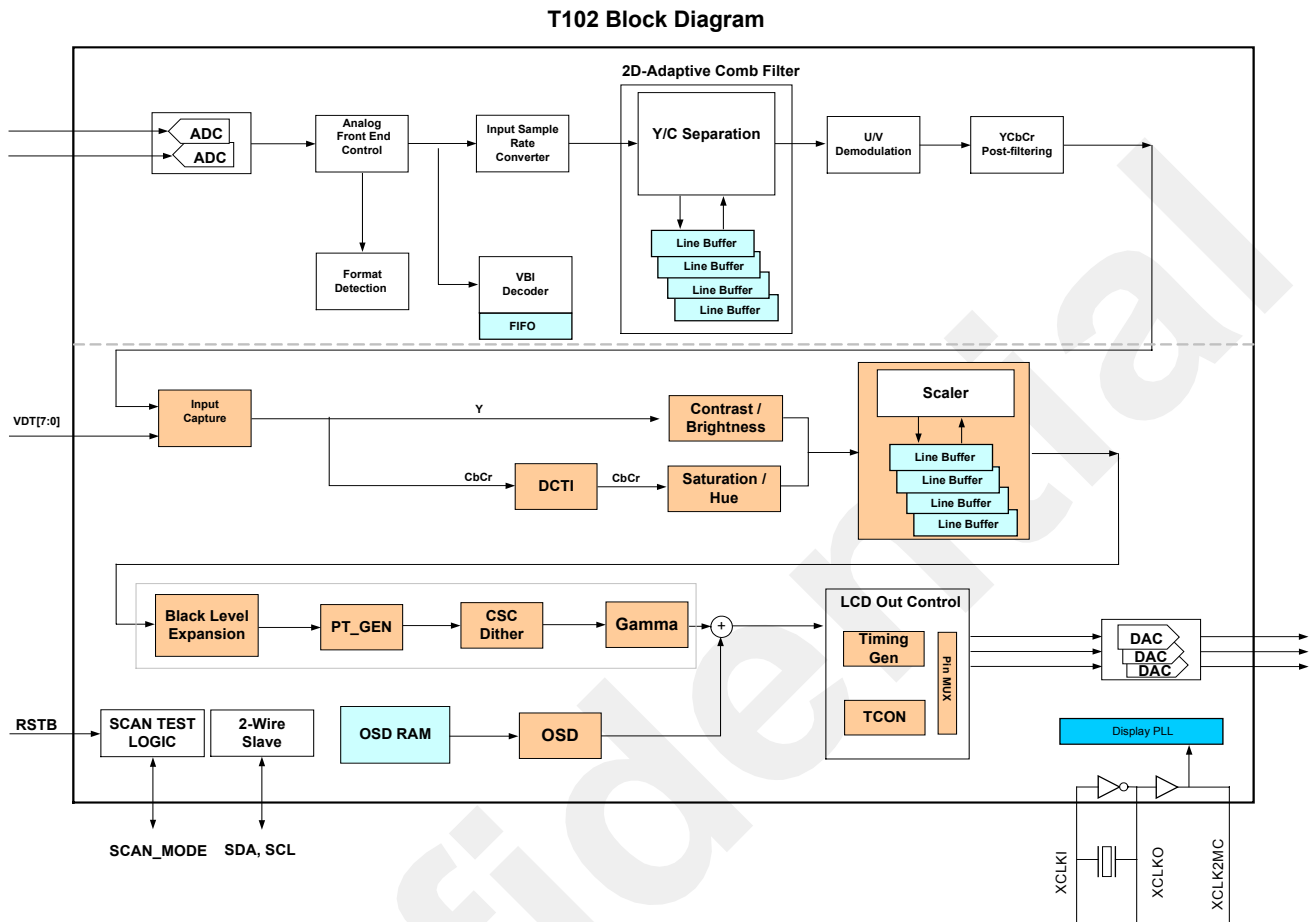


Figure 1-1 System Architecture

1.5 System Configurations

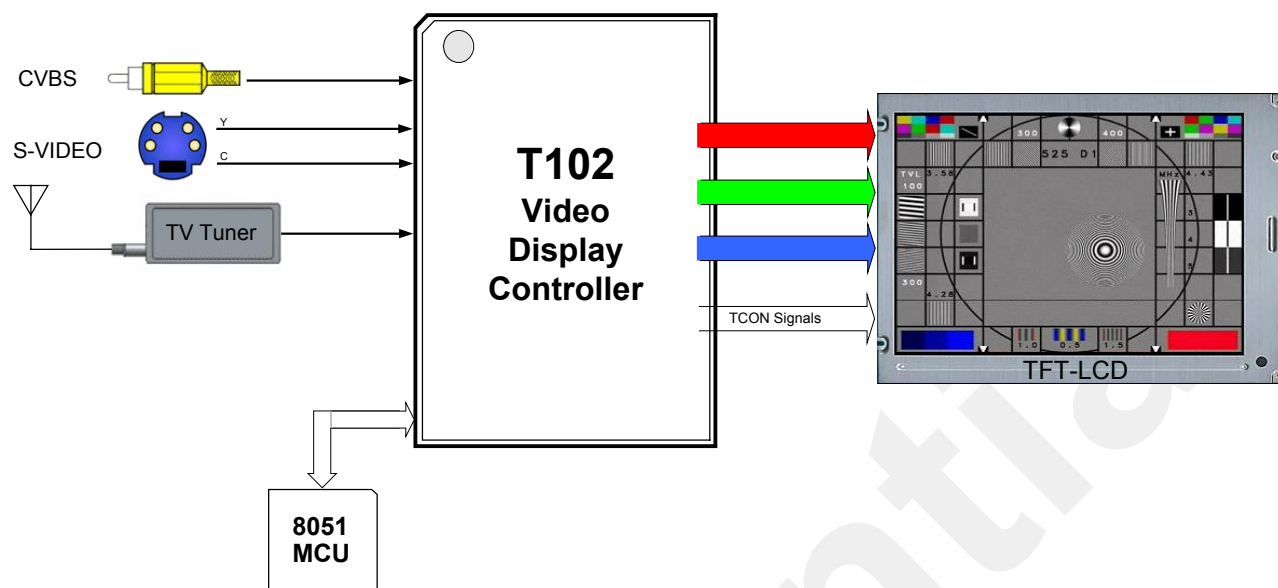


Figure 1-2 System Configurations

1.6 Pinout Diagram

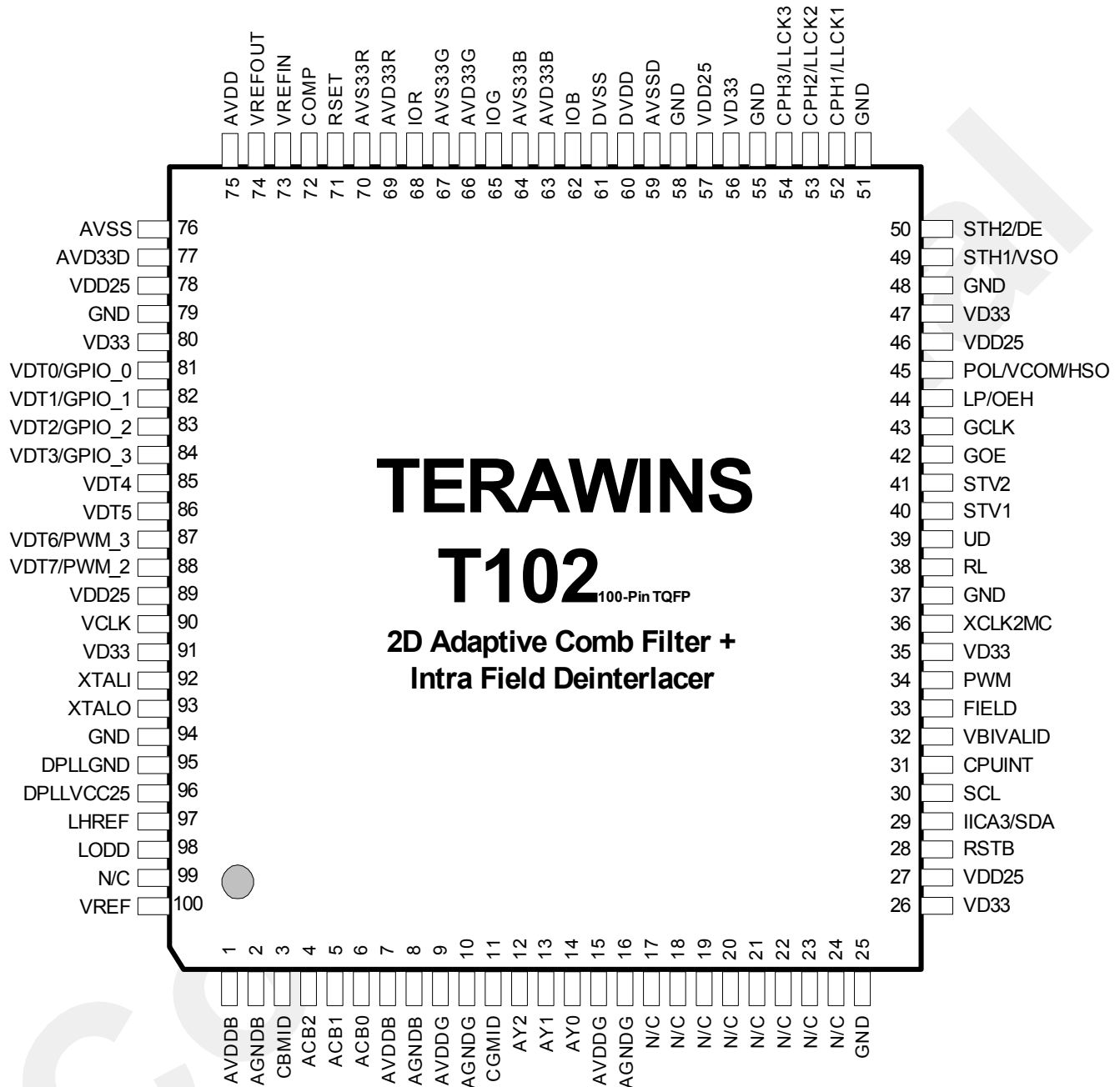


Figure 1-3 Pinout Diagram

1.7 Pin Description

Table 1-1 Pin Description

Symbol	Pin #	Type	Description
Power Supplies			
VDD25	27,46,57,78,89,96	PWR	+2.5V digital core power supply
VD33	26,35,47,56,80,91	PWR	+3.3V digital output power supply
AVDDB	1, 7	PWR	+3.3V analog power supply for ADC channel 2
AVDDG	9, 15	PWR	+3.3V analog power supply for ADC channel 1
GND	25, 37,48,51,55,58,79,94,95	GND	Digital ground
AGNDB	2, 8	GND	Analog ground for ADC channel 2
AGNDG	10, 16	GND	Analog ground for ADC channel 1
AVD33R	69	PWR	+3.3V analog power supply for DAC channel R
AVD33G	66	PWR	+3.3V analog power supply for DAC channel G
AVD33B	63	PWR	+3.3V analog power supply for DAC channel B
AVDD	75	PWR	+2.5V Analog Power Supply for DAC
DVDD	60	PWR	+2.5V Digital Power Supply for DAC
AVD33D	77	PWR	+3.3V Analog Power Supply for DAC I/O pads
AVSS3R	70	GND	Analog ground for DAC channel R
AVSS3G	67	GND	Analog ground for DAC channel G
AVSS3B	64	GND	Analog ground for DAC channel B
AVSS	76	GND	Analog ground for DAC
DVSS	61	GND	Digital ground fro DAC
AVSSD	59	GND	Analog Ground for DAC I/O pads
Output Interface Signals			
IOR	68	AO	Channel R current output
IOG	65	AO	Channel G current output
IOB	62	AO	Channel B current output
LLCK1	52	DO	Output Data Clock
LLCK2	53	DO	Output Data Clock
LLCK3	54	DO	Output Data Clock
VSO	49	DO	Vertical Synchronization Output Control Signal.
HSO	45	DO	Horizontal Synchronization Output Control Signal.
Timing Controller Interface Signals			
STH2	50	DO	Source Driver start pulse
LP	44	DO	Latch pulse for column driver
GCLK	43	DO	Gate driver clock
GOE	42	DO	Gate driver output enable
STV1	40	DO	Gate Driver start pulse
STV2	41	DO	Gate Driver start pulse
UD	39	DO	Panel UP/Down Control
RL	38	DO	Panel Right/Left Control
Q1H	32	DO	Panel Polarity Control
2-wire serial bus Interface Signals			
SCL	30	DI	2-wire serial bus clock. Power down does not affect SCL.

Symbol	Pin #	Type	Description
SDA	29	I/O	2-wire serial bus data. Power down does not affect SDA.
Configuration interface Signals			
CPUINT	31	I/O	Internal Interrupt.
RSTB	28	DI	Whole chip reset. (Internal Pull-up)
Test Pins			
FIB1	99	AO	ADC test pin
FILED	33	DO	Field flag
ADC Interface			
ACB2	4	AI	Analog input 2 of channel 2
ACB1	5	AI	Analog input 1 of channel 2
ACB0	6	AI	Analog input 0 of channel 2
AY2	12	AI	Analog input 2 of channel 1
AY1	13	AI	Analog input 1 of channel 1
AY0	14	AI	Analog input 0 of channel 1
Video-In Interface			
VCLK	90	DI/O	ITU-656 video clock
VDT0	81	DI/O	ITU-656 video port
VDT1	82	DI/O	ITU-656 video port
VDT2	83	DI/O	ITU-656 video port
VDT3	84	DI/O	ITU-656 video port
VDT4	85	DI/O	ITU-656 video port
VDT5	86	DI/O	ITU-656 video port
VDT6	87	DI/O	ITU-656 video port
VDT7	88	DI/O	ITU-656 video port
LHREF	97	DI	ITU-601 video port
LODD	98	DI	ITU-601 video port
PLL Reference Clock			
XTALI	92	DI	Output PLL reference clock input
XTALO	93	DO	Output PLL reference clock output
XCLK2MC	36	DO	Buffered XTALI for external microprocessor.
Power Management Interface Signals			
PWM	34	DO	Pulse Width Modulation for backlight control.
General Purpose Input Output Signals			
GPIO0	81	DI/O	GPIO port 0
GPIO1	82	DI/O	GPIO port 1
GPIO2	83	DI/O	GPIO port 2
GPIO3	84	DI/O	GPIO port 3

2 Theory of Operations

2.1 I²C Command Protocol

Before your tester writes I²C commands to T102, slave address must be set at 50h. The timing sequence can be shown as below. After 4 cycles, the tester can get started IIC commands. SDA(A3) can affect slave address. Set low for 40h. Set high for 50h.

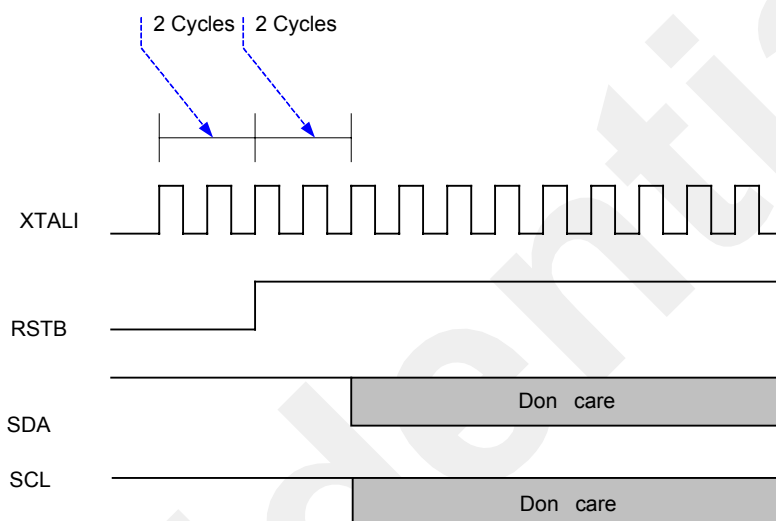


Figure 2-1 Power-up initialization

When tester issues commands to the T102, the only way the user can program the T102 is using the 2-wire serial bus protocol. This section describes the 2-wire serial bus protocol. Data transfers on the 2-wire serial bus are initiated with a START condition and are terminated with a STOP condition. Normal data on the SDA line must be stable during the high period of the SCL. The transition on the SDA is only allowed while SCL is low. The START condition is unique case and is defined by a high-to-low transition on the SDA while the SCL is high. The STOP condition is a unique case and is defined by a low-to-high transition on the SDA while the SCL is high. Each data packet on the 2-wire serial bus consists of 8 bits of data followed by an ACK bit. Data is transferred with MSB first. The transmitter releases the SDA line during the ACK bit and the receiver of data transfer must drive the SDA line low during the ACK bit to acknowledge receipt of the data. The frequency of SCL can be from 50 KHz up to 2 Mhz.

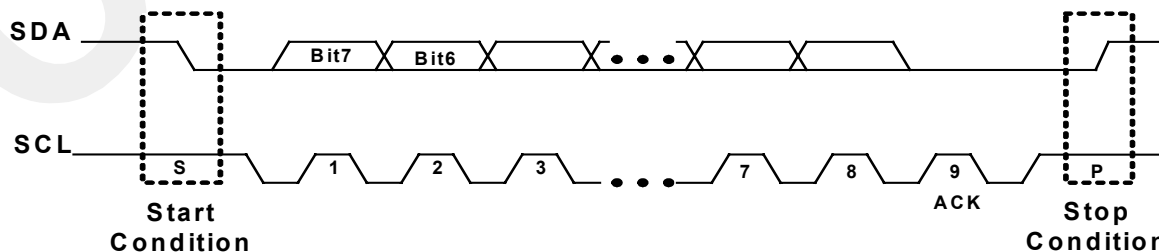


Figure 2-2 2-wire serial bus Protocol

The timing below shows a typical T102 IIC single byte write command,

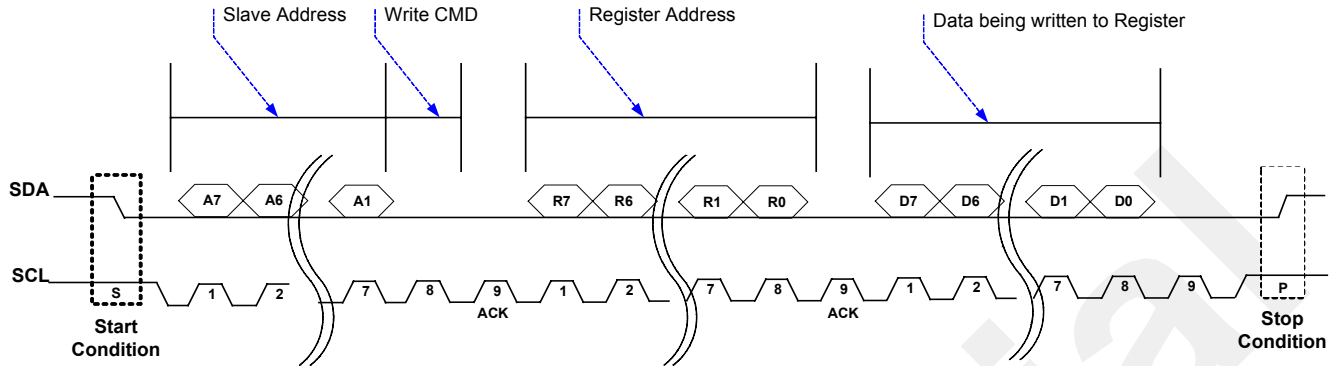


Figure 2-3 T102 IIC single byte write command

The timing below shows a typical T102 IIC single byte read command,

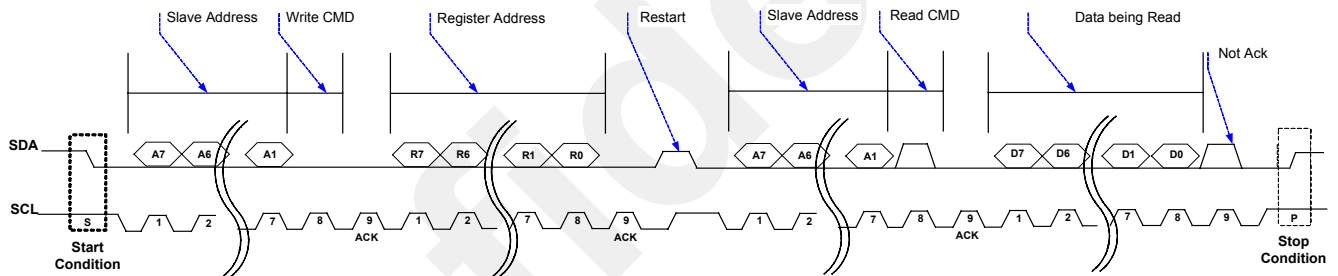


Figure 2-4 T102 IIC single byte read command

2.2 Analog Front End

T102 contains 2 ADCs in Analog Front End. Each channel of ADCs can digitalize SDTV signals from analog to digital. The figure shown below can describe how to select a SDTV signal from 3 inputs prior to ADC.

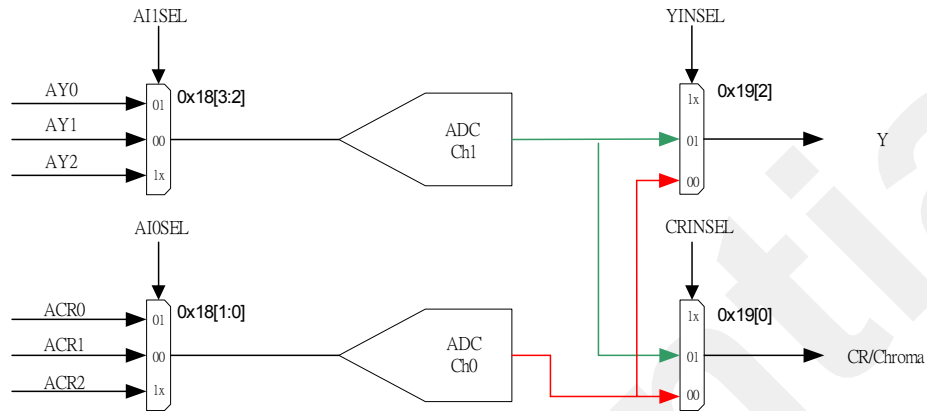


Figure 2-5 Analog Front End

2.3 Y/C Separation and Chroma Decoder

A composite video has luma(Y) and chroma(C) information mixed in the same video signal. This video signal can also be represented by the equation below,

$$CVBS = Y + U * \sin(wt) + V * \cos(wt)$$

Where $w = 2\pi f_{SC}$, $f_{SC} = 3.58\text{Mhz}$ if NTSC, $f_{SC} = 4.43\text{Mhz}$ if PAL

The figure below shows a typical composite signal. The 2-D adaptive comb filter inside T102 is designed to separate Y and C from a composite video signal.

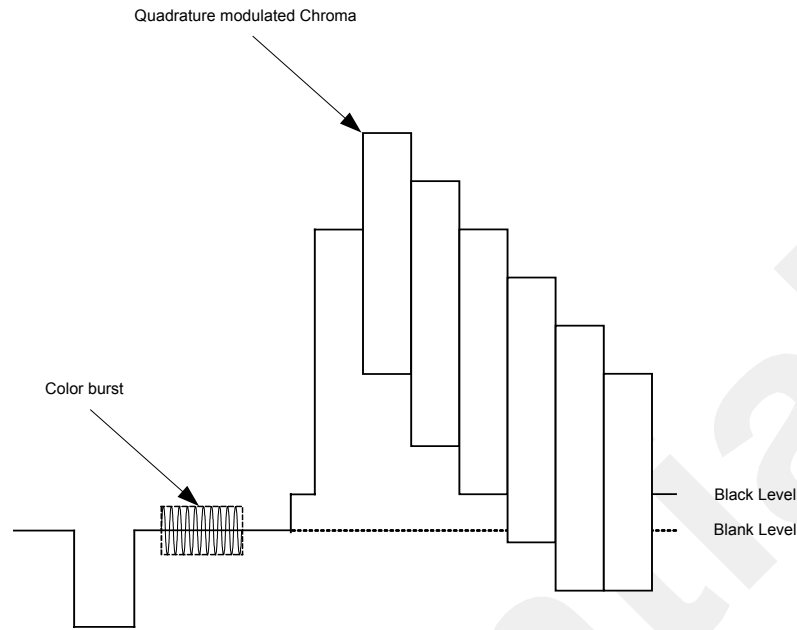


Figure 2-6 Composite Video Signal

. The conventional 3-line comb filter fails to separate Y and C if there is a vertical transition. The 2-D adaptive comb filter is based on equally weighting factors that color changes along vertical and horizontal edges. Let the amount of color change along vertical and horizontal direction DC_v and DCh , the weighting factor can be expressed as following equations,

$$W_h = \frac{DC_v}{DC_v + DCh}$$

$$W_v = \frac{DCh}{DC_v + DCh}$$

By employing adaptive method, chroma can be recovered by following equation,

$$C = Ch * W_h + C_v * W_v$$

After Y/C separation, Y and C should look like waveforms shown as in following figure. Y only contains low frequency part, while C contains high frequency part that is centered around sub-carrier f_{sc} .

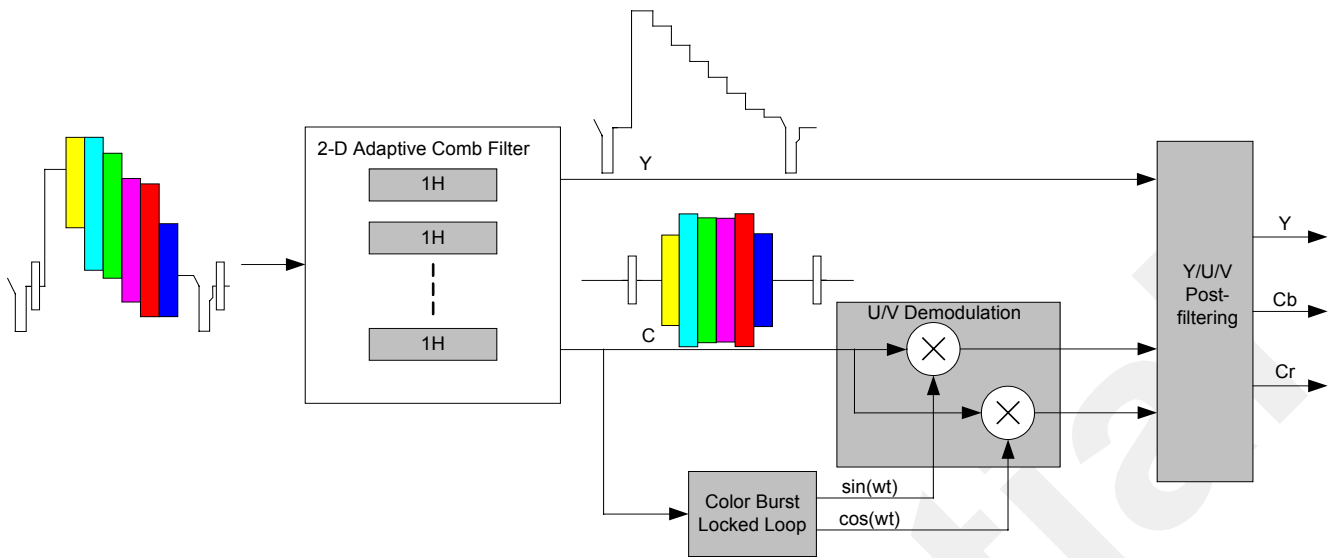


Figure 2-7 Y/C Separation

2.4 Digital Color Transient Improvement (DCTI)

Usually, a composite or S-video SDTV signal may have bandwidth limitation that causes the loss chroma detail around two different color bars. Two pictures shown below illustrate the result before and after DCTI block. Without DCTI (the upper picture), we may see color transient wider than several pixels. A slow transient edge usually blurs image. T102 DCTI algorithm can sharpen those color transient edges. The lower picture shows that chroma data is enhanced by increasing the slope of edge transient without introducing the ring effects.



Figure 2-8 DCTI

2.5 FIR Scaler

FIR Scaler can scale input H/V sizes to fit any LCD panel resolution. The flexible and independent H/V scalers allow users to program display area in 16:9 Full mode, 16:9 non-linear wide mode and 4:3 mode. FIR scaler also provides coefficient-based 2-D sharpness that can sharpen detail of picture.

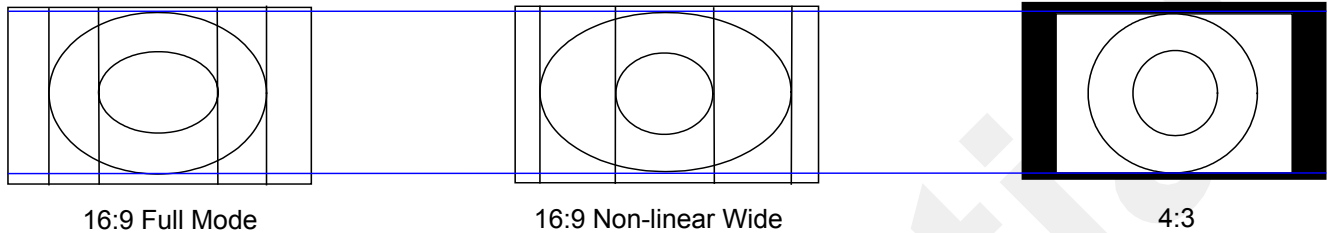


Figure 2-9 Non-Linear Scaling

2.6 Black-Level Extension (BLE)

Black Level Expansion (BLE) can enhance image contrast that makes dark regions of image darker, while bright regions remain unchanged. The figure shown below is BLE transfer function.

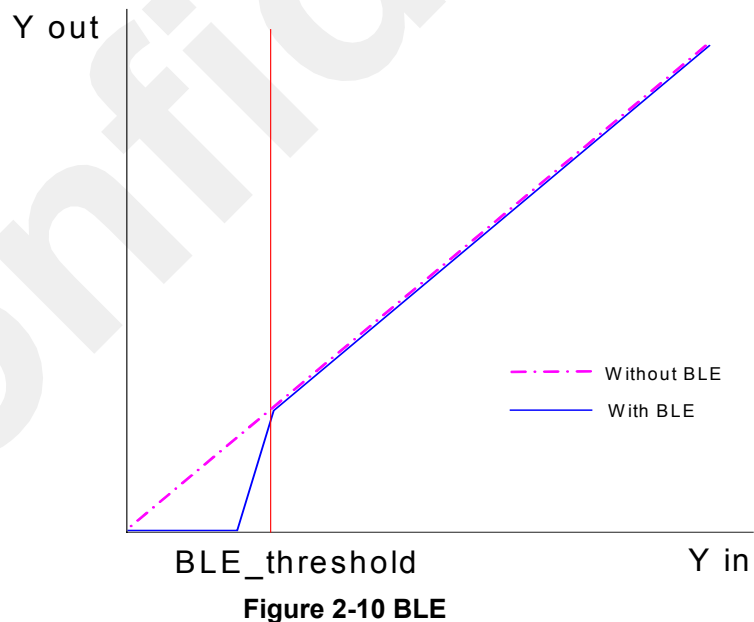


Figure 2-10 BLE

$$Y_{out} = Y_{in} - (Y_{offset} - Y_{in}) * BLE_Gain / 16$$

Where Y_{offset} and BLE_Gain can be programmed by register P0_96h.

2.7 Color Space Converter

A pixel in YCbCr color space can be converted to RGB color space by using following equations,

$$R = YCoefCSC * (Y - 16) + CrCoef_R * (Cr - 128)$$

$$G = YCoefCSC * (Y - 16) - CrCoef_G * (Cr - 128) - CbCoef_G * (Cb - 128)$$

$$B = YCoefCSC * (Y - 16) + CbCoef_B * (Cb - 128)$$

Where $YCoefCSC$ is in 1.7-bit fixed point with default 1.164. $CrCoef_R$ in 1.7-bit fixed point with default 1.596. $CrCoef_G$ in 0.8-bit fixed point with default 0.813. $CbCoef_G$ in 0.8-bit fixed point with default 0.392. $CbCoef_B$ in 2.6-bit fixed point with default 2.017

The equations shown as below correspond to a typical YCbCr-to-RGB converter. In T102, we make those coefficients adjustable.

$$R = 1.164 * (Y - 16) + 1.596 * (Cr - 128)$$

$$G = 1.164 * (Y - 16) - 0.813 * (Cr - 128) - 0.392 * (Cb - 128)$$

$$B = 1.164 * (Y - 16) + 2.017 * (Cb - 128)$$

2.8 Gamma Correction

The relation between input video signal and LCD panel may exist non-linear transfer function such as figure shown below,

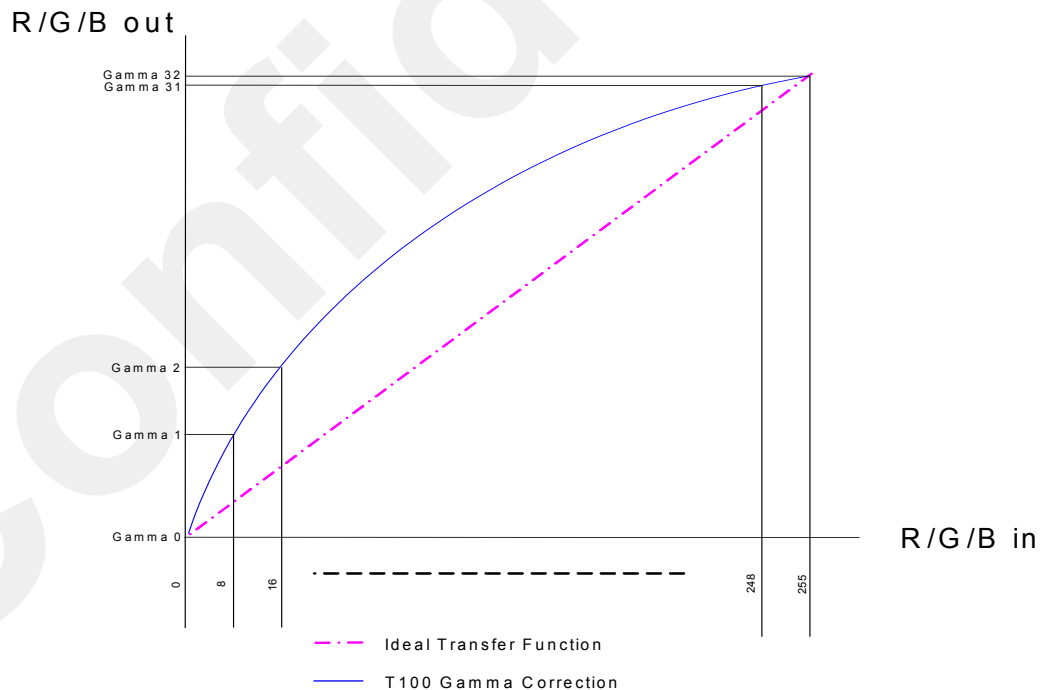


Figure 2-11 Gamma curve

T102 uses 33-point piece-wise linear interpolation instead of RAM-based LUTs. Each point can be programmed via register at P0_93h and P0_94h.

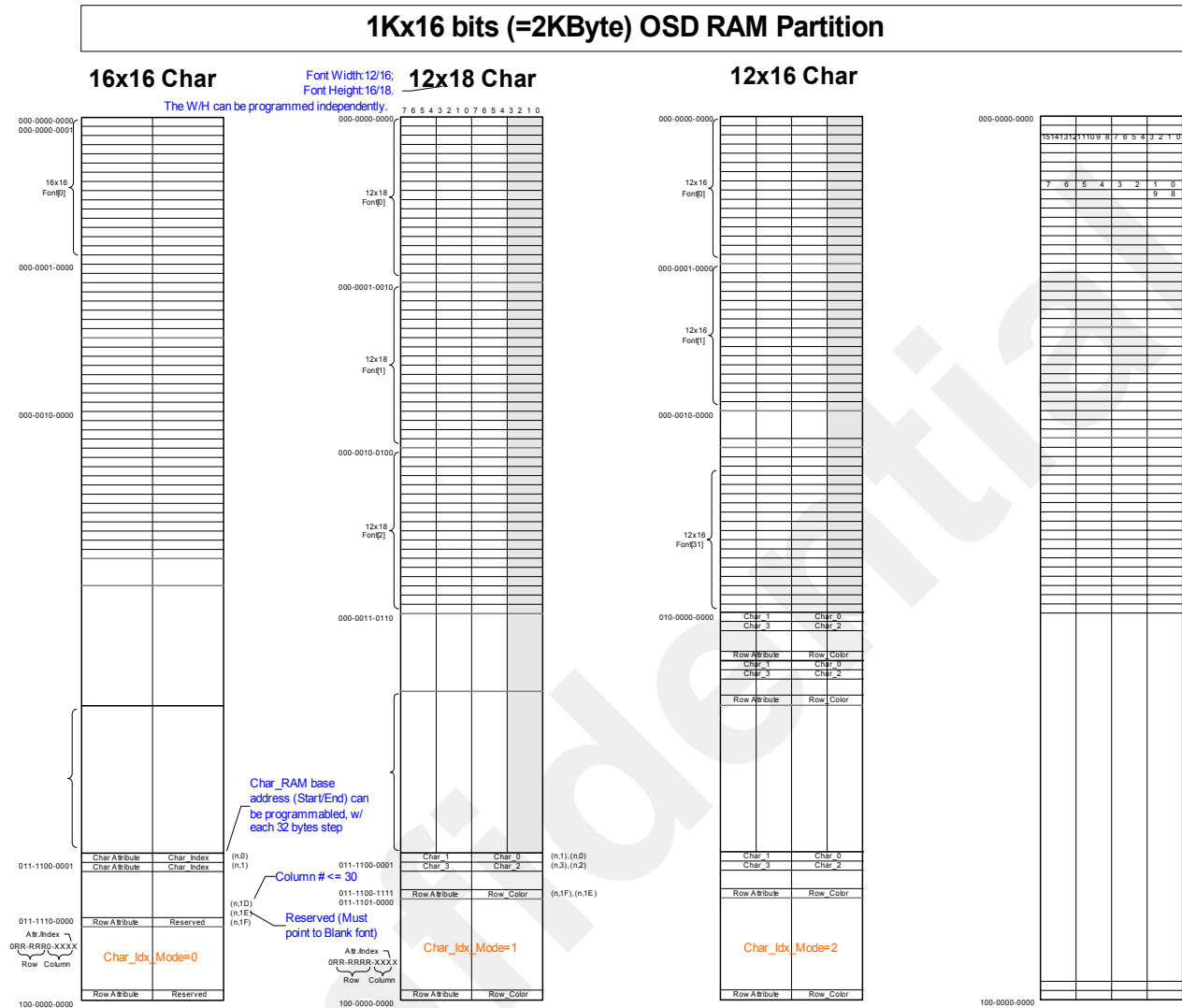
2.9 OSD

2.9.1 OSD Access

Table 2-1 OSD Access

I/O Port	Index	Default	Description
A0h – OSD_Index A1h – OSD_Data	00h	00h	OSD Control Register
	01h	00h	Character Delay_1
	02h	10h	Character Delay_2
	03h	08h	Character Delay_3
	04h	00h	Alpha Blending Control
	05h	38h	Char_RAM Base Address
	06h	40h	Char_RAM Stop Address
	07h	00h	Reserved
	08h	00h	Reserved
	09h	0Ah	Blinking Control
	0Ah	00h	Bit_Map Window Size : Height Upper Bits and BMP Enlarge Control
	0Bh	0Ah	Bit_Map Window Size : Width
	0Ch	66h	Bit_Map Window Size : Height
	0Dh	00h	Reserved
	0Eh	-	OSD LUT RAM data port (Write Only)
	0Fh	00h	Char Control Register
A2h – ORAM_AL		00h	OSD RAM Low Address Port of Starting Access
A3h – ORAM_AH		00h	OSD RAM High Address Port of Starting Access
A4h – ORAM_D		00h	OSD RAM Data Port (Low Byte first, then High Byte). After two Writes, the address will be increased by 1.

2.9.2 RAM Addressing A[10:0]



2.9.3 Character RAM format

In Character Mode (contrast to Bit_Map Mode), the Characters displayed on OSD can be grouped to few rows; each row has its own row attribute which defines the behavior of current character row. And, there is maximum 30 characters in one row, each character has 1~2 bytes to define its character font number and its colors. Due to providing more flexible menu programming, T102 supports three character modes:

Table 2-2 Character Index Modes (Char_idx_Mode)

Char_idx_Mode = 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
				FG[3:0]				Index (Char_0)								XXX-XXX0-0000
				FG[3:0]				Index (Char_1)								XXX-XXX0-0001
				FG[3:0]				Index (Char_2)								XXX-XXX0-0010
				FG[3:0]				Index (Char_29)								XXX-XXX1-1101
				0000b				Index to Blank Char								XXX-XXX1-1110
								CHS	CWS							XXX-XXX1-1111

32 words

Char_idx_Mode = 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
				Index (Char_1)				BG	FG	Index (Char_0)						XXX-XXXX-0000
				Index (Char_3)				BG	FG	Index (Char_2)						XXX-XXXX-0001
				Index (Char_27)				BG	FG	Index (Char_26)						XXX-XXXX-1101
				Index (Char_29)				BG	FG	Index (Char_28)						XXX-XXXX-1110
								CHS	CWS	BG C[2:0]	FG C[3:0]					XXX-XXXX-1111

16 words

Char_idx_Mode = 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
BG	FG[1:0]		Index (Char_1)					BG	FG[1:0]		Index (Char_0)					XXX-XXXX-0000
BG	FG[1:0]		Index (Char_3)					BG	FG[1:0]		Index (Char_2)					XXX-XXXX-0001

BG	FG[1:0]		Index (Char_27)					BG	FG[1:0]		Index (Char_26)					XXX-XXXX-1101
BG	FG[1:0]		Index (Char_29)					BG	FG[1:0]		Index (Char_28)					XXX-XXXX-1110
low BG	Row Gap					CHS	CWS	BG C[2:0]				=> LUT[0]~[3]			XXX-XXXX-1111	

16 words

And the Word #1E_h in Char_idx_Mode=0 is reserved, which must be filled with transparent color and pointed to blank font.

2.9.3.1 Character Index Data (Address to Font Select)

Address Offset: no (part of menu char) Access: Write Only
 Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	WO	00 or BG/FG	Depends on Char_idx_Mode
[4:0]	WO	CHRA[5:0]	Character Address (Index), selects the character font (i.e., 0,1,2,... A,B,C, a,b,c,\$,%,...). If the value is number N, then it selects the N th font, and that font starting address is (N x Font_Height). The Font_Height is defined in OSD_0Fh<5>.

In Char_idx_Mode=0, this Index is 8 bits, and selecting one of total 256 fonts (but OSD RAM is small, for 64 fonts maximum)

In Char_idx_Mode=1, this Index is 6 bits, and selecting one of total 64 fonts

In Char_idx_Mode=2, this Index is 5 bits, and selecting one of total 32 fonts

2.9.3.2 Character Attribute

Address Offset: no (part of menu char) Access: Write Only
 Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	WO	BG_R, BG_G, BG_B	Background R/G/B Color (Intensity=0). If all 0, then no background, i.e. transparent.
[4]	WO	Blink	Enable this Character display with blinking feature. Refer to section 2.9.4.8 for detail blinking control.
[3:0]	WO	FG_R, FG_G, FG_B, FG_I	Foreground R/G/B/Intensity Color. If the value is set as 0000b, then there will be no foreground, i.e. transparent.

2.9.3.3 Row Attribute

Address Offset: no (part of menu char) Access: Write Only
 Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7]	WO	RGAP_BG	Color Select of Row Gap. Set 1 for selecting the same color of background of current row character, 0 for selecting transparent color.
[6:2]	WO	RGAP[4:0]	Row Gap (=Row Space). Inserted range is 4 x (31 _d ~0) scan lines before current Row.
[1]	WO	CHS	Character Height Select. Set 1 for double height, 0 for single height.
[0]	WO	CWS	Character Width Select. Set 1 for double width, 0 for single width. When set to 1, only the even numbered characters will be shown, odd numbered characters are skipped.

2.9.4 OSD Configuration Register

2.9.4.1 Cfg_00h – OSD Control Register

Address Offset: OSD_00h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	OSD_En	Enabling the OSD function. Set 1 for enabling, 0 for disabling OSD
[6]	R/W	Bit_Map	Select Bit Mapped OSD display mode. Set 1 for Bit_Map Mode, 0 for Character Mode.
[5]	R/W	Bit2PP	Two bits per Pixel for Bit_Map mode. Set 1 for 2 Bits/Pixel, 0 for 1 Bit/Pixel.
[4:3]	RO	Reserved	
[2]	R/W	Early_hDE	let OSD a little shift left.
[1]	R/W	Font_Hx2	Character mode, fonts height double.
[0]	R/W	Font_Wx2	Character mode, fonts width double.

2.9.4.2 Cfg_01h – Character Delay_1

Address Offset: OSD_01h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:4]	R/W	VERTD[10:8]	Vertical Starting Position (Upper bits) of Character displaying. These bits with Cfg_03h, total 11 bits, become 2048 steps, with an increment one pixel per step for each field.
[3]	RO	Reserved	
[2:0]	R/W	HORD[10:8]	Horizontal Starting Position (Upper bits) of Character displaying. These bits with Cfg_02h, total 11 bits, become 2048 steps, with an increment one pixel per step.

2.9.4.3 Cfg_02h – Character Delay_2

Address Offset: OSD_02h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HORD[7:0]	Horizontal Starting Position (Lower bits) of Character displaying. These bits with Cfg_01h<2:0>, total 11 bits, become 2048 steps, with an increment one pixel per step.

2.9.4.4 Cfg_03h – Character Delay_3

Address Offset: OSD_03h Access: Read/Write
Default Value: 08h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VERTD[7:0]	Vertical Starting Position (Lower bits) of Character displaying. This register with Cfg_01h<6:4>, total 11 bits become 2048 steps, with an increment one line per step for each field.

2.9.4.5 Cfg_04h – Alpha Blending Control

Address Offset: OSD_04h
Default Value: 00h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	FG_NoAB	OSD Character ForeGround portion will be exclusive to be blended if set to one. Default is 0 as no matter the current displayed pixels are in Character foreground or border/shadow or background or in OSD window, all will be alpha blended with original Video source.
[6:3]	RO	Reserved	
[2:0]	R/W	AB_Set[2:0]	Alpha Blending percentage (n/8). If set 000b, alpha blending is disabled ($0/8 * \text{Original Video Source} + 8/8 * \text{OSD display}$); If set 001b, blending as $1/8 * \text{Original Video Source} + 7/8 * \text{OSD display}$; ... If set N, blending as $N/8 * \text{Original Video Source} + (8-N)/8 * \text{OSD display}$;

2.9.4.6 Cfg_05h – Char_RAM Base Address

Address Offset: OSD_05h
Default Value: 38h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	CharBA[6:0]	Programmable Character RAM Base Address. Those 7 bits become 128 steps, each step is 32 Bytes (one Character Row include Char_Index, Char_Attr, Row_Attr; i.e. 30 column maximum for each Row). The actual address will be 0RR-RRRX-XXXX (in Char_idx_Mode=0 and the CharBA[0] should be 0), or 0RR-RRRR-XXXX (for Char_idx_mode=1 or 2). The RR-RRRR means the value of CharBA[6:0]; the X-XXXX is the nth Char Column. For trading off Font number and Character number in a single RAM (this version is 1Kx16 bits), user should carefully setting this register.

2.9.4.7 Cfg_06h – Char_RAM Stop Address

Address Offset: OSD_06h
Default Value: 40h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	CharEA[6:0]	Programmable Character RAM Stop/End Address (Available if Revision ID $\geq 0h$). Those 7 bits become 128 steps, each step is 32 bytes. The actual stop address will be 0RR-RRRX-XXXX (The RRRR-RRR means the value of CharEA[6:0]; the X-XXXX is the nth Char Column. and OSD will be displayed for Character Row \geq CharBA and $<$ CharEA.

2.9.4.8 Cfg_09h – Blinking Control

Address Offset: OSD_09h
Default Value: 0Ah

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	En_Global_Blink	Enable whole OSD Characters blinking if set to 1.
[6:4]	RO	Reserved	
[3:2]	R/W	BCLK[1:0]	Blinking Frequency Select (internal 4x BCLK for Blinking State Machine). Set 00b for Refresh Rate /16; 01b for 1/32; 10b for 1/64; 11b for 1/128.
[1:0]	R/W	Duty[1:0]	For adjusting the blinking duty cycle, Set: 00b for Global Blink Off, i.e., 0% Background, 100% OSD. 01b for 25% Background, 75% OSD. 10b for 50% Background, 50% OSD. 11b for 75% Background, 25% OSD.

2.9.4.9 Cfg_0Ah – Bit_Map Window Size: Height Upper Bits

Address Offset: OSD_0Ah
Default Value: 00h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:4]	R/W	BMH[9:8]	Bit Map Window Height Upper bits (only available in Bit_Map mode). Please refer to OSD_0Ch for detail. User must be careful of the OSD RAM size limitation.
[3:2]	R/W	BMP_Height_xN [1:0]	Bit Map Window Vertical Enlarge (only available in Bit_Map mode). Set 00b for 1 line per dot, 01b for 2 lines per dot, 10b for 3 lines per dot, 11b for 4 lines per dot.
[1:0]	R/W	BMP_Width_xN[1:0]	Bit Map Window Horizontal Enlarge (only available in Bit_Map mode). Set 00b for 1 pixel per dot, 01b for 2 pixels per dot, 10b for 3 pixels per dot, 11b for 4 pixels per dot.

2.9.4.10 Cfg_0Bh – Bit_Map Window Size: Width

Address Offset: OSD_0Bh
Default Value: 0Ah

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BMW[7:0]	Bit Map Window Width Lower bits (only available in Bit_Map mode). This register has 8 bits, i.e., 256 steps (value 00h is not valid), each step is 16 or 8 dots depends on Bit2PP (OSD_00h<5>) setting. When Bit2PP=0 (i.e., 1 bit/pixel), each step is 16 dots. When Bit2PP=1 (i.e., 2 bits/pixel), each step is 8 dots. User must be careful of the OSD RAM size limitation.

2.9.4.11 Cfg_0Ch – Bit_Map Window Size: Height

Address Offset: OSD_0Ch Access: Read/Write
 Default Value: 66h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BMH[7:0]	Bit Map Window Height Lower bits (only available in Bit_Map mode). This register combined with OSD_0Ah<5:4> and become 10 bits, i.e. 1024 height step: all 0 for reserved, 10'h001 for 1 line, 10'h3FF for 1023 lines. User must be careful of the OSD RAM size limitation.

2.9.4.12 Cfg_0Eh – OSD Color LUT RAM Data Port

Address Offset: OSD_0Eh Access: Write Only
 Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	LUT_D[7:0]	The data will be written to (or read from) OSD Color LUT RAM. After each Read or Write access to LUT RAM, then the LUT address will be increased automatically.

Note: Whenever the Configuration Index is programmed from other index value to 0Eh, the OSD Color LUT RAM becomes access capable and the address pointer is reset to 1 (the starting byte). In other words, whenever the index value is programmed to non-0Eh value, the OSD Color LUT RAM can not be access, and the pointer always kept at 1.

Note: The order to fill LUT RAM is:

1. LUT[1]_Green/Blue
2. LUT[1]_0000b/Red
3. LUT[2]_Green/Blue
4. LUT[2]_0000b/Red
5. LUT[3]_Green/Blue
6. ----
29. LUT[15]_Green/Blue
30. LUT[15]_0000b/Red
31. LUT[0]_Green/Blue (wrap to beginning)
32. LUT[0]_0000b/Red
33. LUT[1]_Green/Blue
34. LUT[1]_0000b/Red
-

2.9.4.13 Cfg_0Fh – OSD Color LUT RAM Data Port

Address Offset: OSD_0Fh Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5]	R/W	FontH_18	Set to 1 for font height being 18, else 16
[4]	R/W	FontW_16	Set to 1 for font width being 16, else 12
[3:2]	R/W	Char_Idx_Mode[1:0]	Character attribute/Index coding modes, 0 for original 2 bytes (256 index) mode, 1 for 1-byte (64 index) mode, 2 for 1-byte (32 index) mode, 3 for reserved.
[1:0]	R/W	CRAM_ByteAccess[1:0]	OSD RAM access pointer behavior: 0X: Word (2-bytes) R/W; (Fonts, BMP, Character Menu) 10: Low byte only; 11: High byte only; (Character Menu)

2.9.5 Functional Description

2.9.5.1 Host Access OSD RAM

2.9.5.1.1 Writing Data

The OSD RAM size is 1Kx16, i.e., 1K word with each word is 2 bytes. The host interface is 8-bit data width, so whenever the host writes 2 times (one for data low byte, the other for data high byte) then it becomes one write with 16-bit data to OSD RAM.

The ORAM_D (OSD module base address + 04h) port when writing in the 1st/3rd/5th/7th ... times, it will latch lower byte of OSD RAM writing data when the host want to program Font or Character, Attribute, BMP values; and when writing 2nd/4th/6th/8th ... times, it will use this 8bits data as high byte and write both two bytes to OSD RAM.

2.9.5.1.2 Reading Data

Read back data in OSD RAM is disabled.

2.9.5.1.3 Access Address

The OSD RAM access pointer is programmed by the host write access to ORAM_AL and ORAM_AH ports. The OSD RAM size is 1Kx16, so the pointer is required to cover 1K words, i.e., 11 address lines => A[10:0]. When the host read these ORAM_AL/ORAM_AH ports, the pointer value reflects the current OSD RAM accessing pointer.

2.9.5.2 OSD Displaying in Character Mode

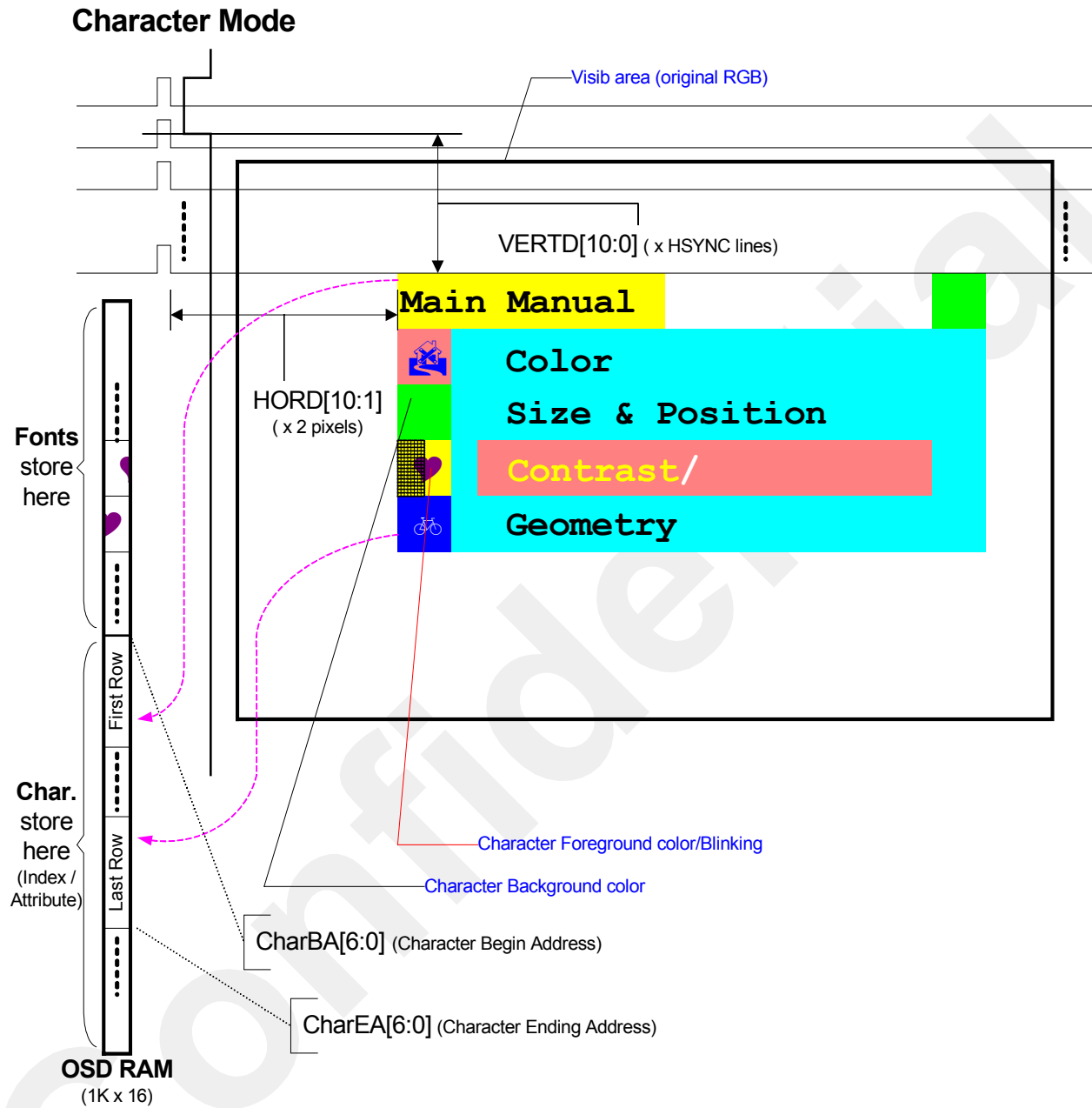
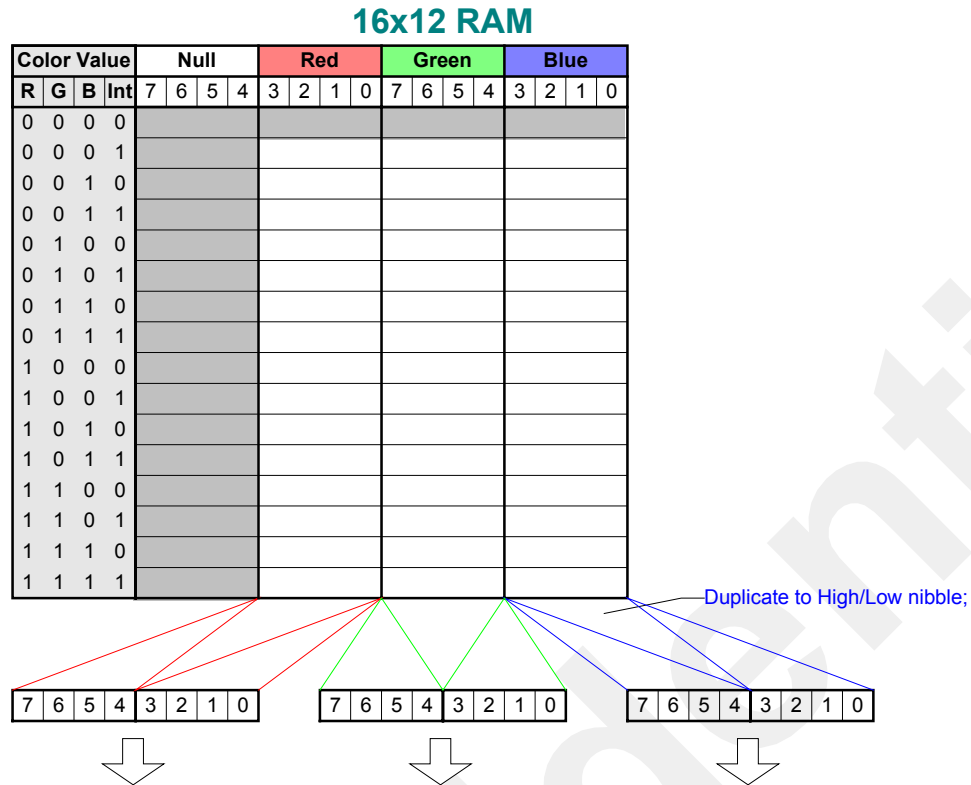


Figure 2-13 OSD Character Mode

2.9.5.3 OSD LUT Color Mapping



1. Character Mode

1. Char_idx_Mode=0, FG[3:0] as Color_0= transparent; Color_1~15= LUT[1..15]
BG[2:0] as Color_0= transparent; Color_1~7= LUT[2,4,..14]
2. Char_idx_Mode=1, FG as Color_0= transparent; Color_1= depends on its Row_Attribute FG_C[3:0], then redirect to transparent or LUT[1..15]
BG as Color_0= transparent; Color_1= depends on its Row_Attribute BG_C[2:0], then redirect to transparent or LUT[2,4,..14]
3. Char_idx_Mode=2, FG[1:0] as Color_0= transparent; Color_1~3= LUT[1..3]
BG as Color_0= transparent; Color_1= depends on its Row_Attribute BG_C[2:0], then redirect to transparent or LUT[2,4,..14]

2. Bit_Map Mode

- 1 Bit/Pixel mode: Color_0= transparent; Color_1= LUT[1]
- 2 Bits/Pixel mode: Color_0= transparent; Color_1~3= LUT[1..3]

Figure 2-14 OSD Color Look Up Table

2.9.5.4 Programming Examples

2.9.5.4.1 Configuring OSD Function

To access OSD configuration registers, write register index to port A0h, and read/write data from port A1h. For example, set :

```
IOW    A0h, 05h      ; point to OSD_05h (Char Base Address register).
IOR     A1h;          ; get Char Base Address.
IOW    A0h, 06h      ; point to OSD_06h (Char Stop Address register).
IOW    A1h, 3Eh;      ; Set Char Stop Address of current menu.
```

2.9.5.4.2 Fill LUT RAM

LUT RAM size is 16 (address) x 12 (width). For example, need to fill LUT RAM as:

LUT_RAM[1]=F5Ah, ...LUT_RAM[15]=EF0h

```
IOW    A0h, 0Eh      ; point to OSD_0Eh (LUT RAM Data port), this will let LUT RAM be
                      ; access-able and pointer starts from 0h of LUT RAM.
IOW    A1h, 5Ah;      ; fill Green = 0101b and Blue = 1010h in LUT_RAM[1].
IOW    A1h, 0Fh;      ; fill Red = 1111b in LUT_RAM[1].
                      ; after this write, h/w will increase LUT RAM address to 2 automatically
.....
IOW    A1h, F0h;      ; fill Green = 1111b and Blue = 0000h in LUT_RAM[15].
IOW    A1h, 0Eh;      ; fill Red = 1110b in LUT_RAM[15].
                      ; after this write, h/w will increase LUT RAM address to 0 automatically
IOW    A0h, non-0Eh   ; Disable LUT RAM programming.
```

2.9.5.4.3 Load Fonts to OSD RAM

OSD RAM size is 1K (address: 000h ~ BFFh) x 16 (width). Fonts storing starts from address 000h. For example, loading some fonts to OSD RAM as:

Font[0] is a space (all zero), Font[1] is a character 2 with box, Font[14] is a graphic,...

```
IOW    A2h, 00h      ; set OSD RAM starting access address low byte. (bit [7:0] as A[7:0])
IOW    A3h, 00h;      ; set OSD RAM starting access address high byte. (bit [3:0] as A[11:8])
                      ; then the OSD RAM address pointer is set to 000h.
IOW    A4h, 00h;      ; low byte of first row of Font[0].
IOW    A4h, 00h;      ; high byte of first row of Font[0], after this write, h/w will increase OSD
                      ; RAM address to 1 automatically
IOW    A4h, 00h;      ; low byte of 2nd row of Font[0].
IOW    A4h, 00h;      ; high byte of 2nd row of Font[0], after this write, h/w will increase OSD
                      ; RAM address to 2 automatically
..... (for example, programmed font size is 18 (height) x 12 (width)
IOW    A4h, 00h;      ; low byte of 18th (last) row of Font[0].
IOW    A4h, 00h;      ; high byte of 18th row of Font[0], after this write, h/w will increase OSD
                      ; RAM address to 012h automatically
IOW    A4h, F0h;      ; low byte of first row of Font[0]. (since font width is 12, the low byte bit[3:0]
                      ; is no use)
IOW    A4h, FFh;      ; high byte of first row of Font[0], after this write, h/w will increase OSD
                      ; RAM address to 013h automatically
.....
IOW    A2h, 68h      ; set OSD RAM starting access address low byte. (bit [7:0] as A[7:0])
IOW    A3h, 01h;      ; set OSD RAM starting access address high byte. (bit [3:0] as A[11:8]),
                      ; then the OSD RAM address pointer is set to 168h = 14d * 18d.
IOW    A4h, 40h;      ; low byte of first row of Font[14].
IOW    A4h, A3h;      ; high byte of first row of Font[14],
```

2.10 TCON

2.10.1 LCD Panel Pin Assignment

In this section, we illustrate those pins connected to AU 7" TFT-LCD panel module in a T102 video system.

Table 2-3 T102 Rotation Control and LCD Panel Scanning Direction

L/R	U/D	STH	STV	Reg 0xE1	Scanning Direction
1	1	STH2	STV1	0xBC	Down-to-up, left-to-right
1	0	STH2	STV2	0xF4	Up-to-down, left-to-right
0	1	STH1	STV1	0xA8	Down-to-up, right-to-left
0	0	STH1	STV2	0xE0	Up-to-down, right-to-left

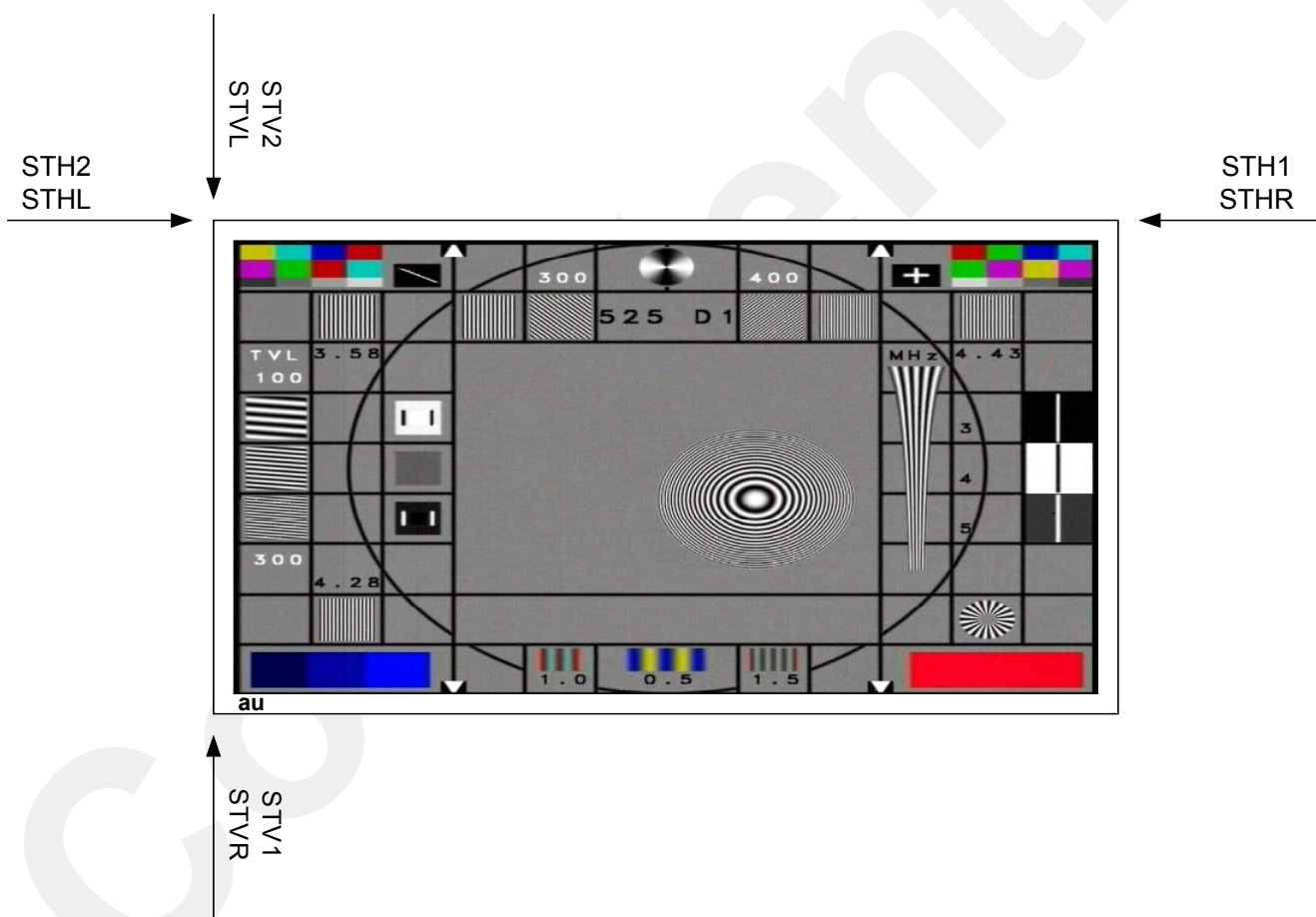


Figure 2-15 Scanning Direction of AU 7" panel

2.10.2 TCON Timing

T102 is designed for analog LCD panel. Each 24-bit color pixel must be converted into analog voltage via built-in triple DACs. The table 2-1 shows a typical setting for AU 7" panel with 10-Mhz operation clock.

Table 2-4 T102 TCON Register Set (C8 =1Bh, C9=03, CA=03h)

Reg	Reg value	Operation
0x20	0x21	Line-inverted Control
0x21	0x79	Polarity Control
0x23,0x22	0x022D	Placement of OEH
0x24	0x0C	Duration of OEH
0x26,0x25	0x024B	Placement of POL
0x28,0x27	0x021C	Placement of GCLK
0x2A,0x29	0x0029	Duration of GCLK
0x2B	0x01	Placement of STH
0x30	0x01	Enable Placement of STV
0x32,0x31	0x01FB	Placement of GOE
0x34,0x33	0x0037	Duration of GOE
0x35	0x06	Placement of STV

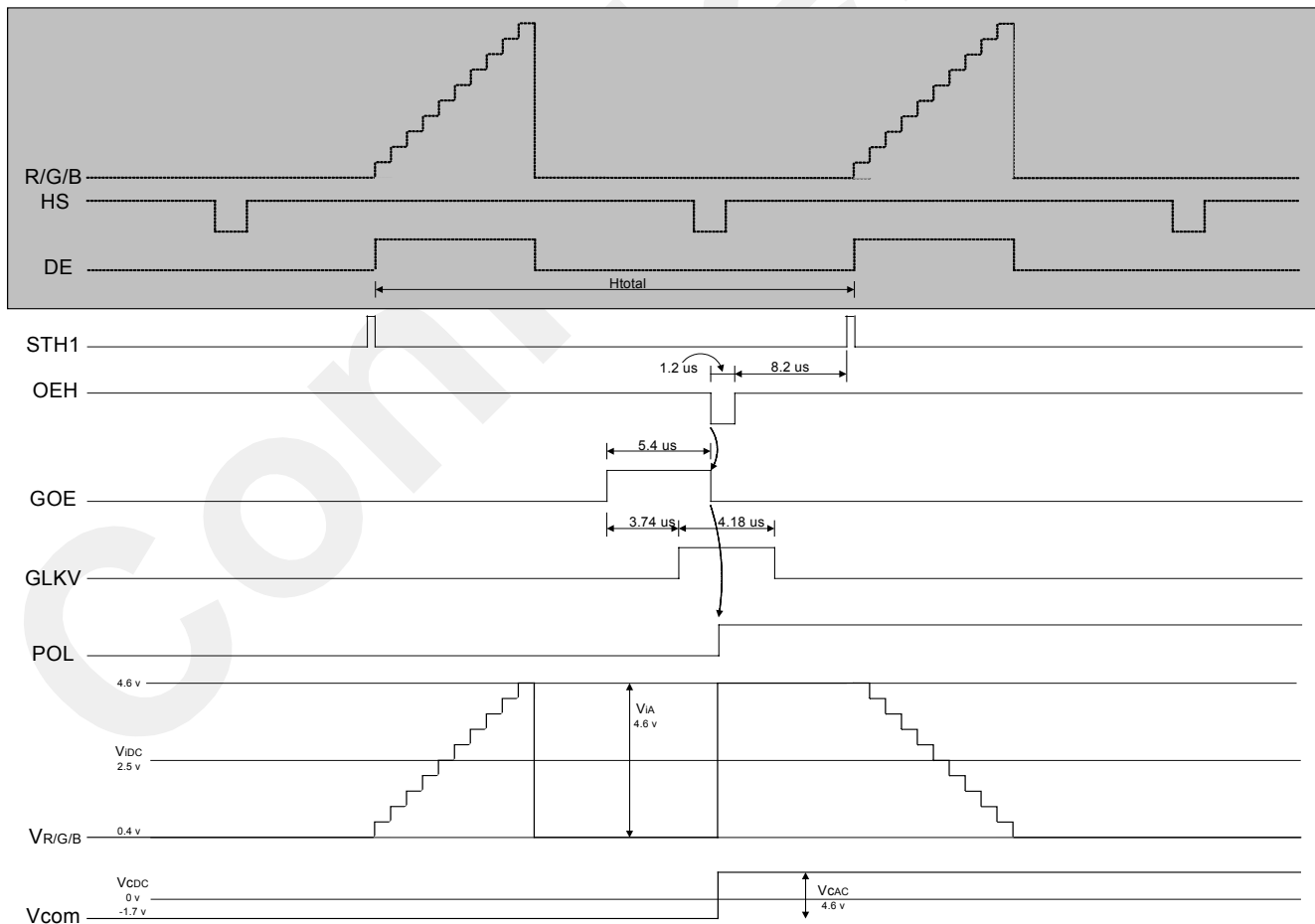


Figure 2-16 AU 7" TCON Timing Spec

The waveforms shown below illustrate TCON location counting. Each TCON signal's placement and duration are allowed to program as alike as analog LCD panels require. On the figure 2-2, the pulse placement starts counting at the leading edge of DE. After placement counter meets the value we give to {P1_27h,P1_28h}, the duration counter starts to count until the duration meets {P1_29h,P1_2Ah}. All of location counting use LLCK as counter clock.

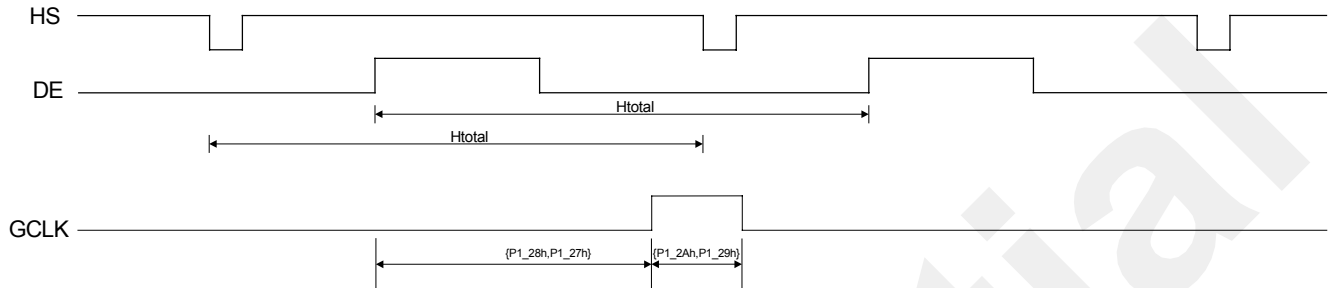


Figure 2-17 Location Counting of GCLK

3 Register Description

Serial Bus Register Set Page 0

3.1 ADC Register Set

3.1.1 ADC Channel 0 Current Register

Address Offset: 00h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	
[3:0]	R/W	IR	ADC channel 0 current strength

3.1.2 ADC Channel 1 Current Register

Address Offset: 01h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	IG	ADC channel 1 current strength

3.1.3 ADC Channel 0 Static Gain

Address Offset: 07h Access: Read/Write
Default Value: FFh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ADCRSG	This register can set a fixed gain for ADC channel 0 when static gain control is enabled

3.1.4 ADC Channel 1 Static Gain

Address Offset: 08h Access: Read/Write
Default Value: FFh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ADCGSG	This register can set a fixed gain for ADC channel 1 when static gain control is enabled

3.1.5 ADC ACR Channel Offset

Address Offset: 0Ah Access: Read/Write
Default Value: 60h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_ROFF	ADC Channel 0 DC Offset Control
[1:0]	R/W	RESERVED	

3.1.6 ADC AY Channel Offset

Address Offset: 0Bh Access: Read/Write
Default Value: 60h Size: 8 bits

Bit	Access	Symbol	Description
-----	--------	--------	-------------

[7:2]	R/W	ADC_GOFF	ADC Channel 1 DC Offset Control
[1:0]	R/W	RESERVED	

ADC General Control Configuration Register

Address Offset: 0Dh

Access: Read/Write

Default Value: 20h

Size: 8 bits

	Access	Symbol	Description						
[7]		RESERVED							
[6]	R/W	CLPMD	Clamping mode <table><tr><th>Mode</th><th>Type</th></tr><tr><td>0</td><td>Fixed window</td></tr><tr><td>1</td><td>Locked Window</td></tr></table>	Mode	Type	0	Fixed window	1	Locked Window
Mode	Type								
0	Fixed window								
1	Locked Window								
[5]	R/W	DCEN	DC Clamping Enable						
[4]	R/W	DCSEL	Clamping Source Selection						
[3]		RESERVED							
[2]	R/W	DC_CAL_RDY	DC Calibration Ready						
[1]	R/W	DC_CALEN	DC Calibration Enable						
[0]	R/W	DC_CALMD	DC Calibration Mode <table><tr><th>Mode</th><th>Type</th></tr><tr><td>0</td><td>minimum</td></tr><tr><td>1</td><td>average</td></tr></table>	Mode	Type	0	minimum	1	average
Mode	Type								
0	minimum								
1	average								

3.1.7 ADC Gain ReadBack

Address Offset: 0Eh

Access: Read Only

Default Value: -

Size: 6 bits

Bit	Access	Symbol	Description
[7:0]	R	adc_auto_gain	ADC automatic gain control read back.

3.1.8 ADC Power Down Control

Address Offset: 0Fh

Access: Read/Write

Default Value: 00h

Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5]	R/W	PD1	1: Power down 0: Power up
[4]	R/W	PD0	1: Power down 0: Power up
[3:0]	R/W	RESERVED	

3.1.9 YPbPr Clamping Control Register

Address Offset: 11h

Access: Read/Write

Default Value: 00h

Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	R/W	RESERVED	

[1]	R/W	GSCALE	ADC Channel 1 Clamping Mode	
			Mode	Select
			0	Clamp to ground
			1	Clamp to midscale
[0]	R/W	RSCALE	ADC Channel 0 Clamping Mode	
			Mode	Type
			0	Clamp to ground
			1	Clamp to midscale

3.1.10 Analog Source MUX Selection

Address Offset: 18h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:2]	R/W	AI1SEL	Analog mux selection for ADC channel 1 00: AY1 01: AY0 1x: AY2
[1:0]	R/W	AI0SEL	Analog mux selection for ADC channel 0 00: ACB1 01: ACB0 1x: ACB2

3.1.11 Y/Cb/Cr Data Switching Control

Address Offset: 19h Access: Read/Write
 Default Value: 07h Size: 8 bits

Bit	Access	Symbol	Description						
[7:3]	R/W	RESERVED							
[2]	R/W	YINSEL	The digitized Y or Composite data can be taken from one of 3 ADCs according to following table <table><tr><th>Mode</th><th>Type</th></tr><tr><td>0</td><td>ADC Ch0</td></tr><tr><td>1</td><td>ADC Ch1</td></tr></table>	Mode	Type	0	ADC Ch0	1	ADC Ch1
Mode	Type								
0	ADC Ch0								
1	ADC Ch1								
[1]		RESERVED							
[0]	R/W	CRINSEL	The digitized CR or Chroma data can be taken from one of 3 ADCs according to following table <table><tr><th>Mode</th><th>Type</th></tr><tr><td>0</td><td>ADC Ch0</td></tr><tr><td>1</td><td>ADC Ch1</td></tr></table>	Mode	Type	0	ADC Ch0	1	ADC Ch1
Mode	Type								
0	ADC Ch0								
1	ADC Ch1								

3.1.12 ADC Analog AGC Selection

Address Offset: 1Ah Access: Read/Write
 Default Value: 42h Size: 8 bits

Bit	Access	Symbol	Description
-----	--------	--------	-------------

Bit	Access	Symbol	Description
[7:6]	R/W	AGC_GAINMD	Mode
			Type
			0 Positive gain
			1 Positive gain 1x~2x
			2 Negative gain 1x~2x
			3 Negative gain
[5:2]	R/W	RESERVED	
[1]	R/W	Y_AGC_SEL	If 0, refer to ADCGSG
			Mode
			Type
			0 Static gain
			1 Dynamic gain
[0]	R/W	CR_AGC_SEL	If 0, refer to ADCRSG
			Mode
			Type
			0 Static gain
			1 Dynamic gain

3.1.13 Blank Sync Level

Address Offset: 1Ch
Default Value: F0h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BLANK_SL	

3.1.14 De-Interlaced Process & Vertical Shadow Control Register

Address Offset: 30h
Default Value: 82h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	CBCR_INTERP	1: Enable CbCr interpolation (default) 0: Disable
[6]	R/W	RESERVED	
[5]	R/W	VST_CHGSEL	1: Vsync timing change determined by 8*# of XCLK 0: Vsync timing change determined by # of hsync (default) # can be assigned at Reg 0x3A
[4]	R/W	INT_EDGE	Interrupt polarity 1: positive 0: negative (default)
[3]	R/W	LB_SIZE_FIXED	This bit control capture size for Scaler. 1: Hsize and Vsize are assigned by 54h ~57h 0: sizes assigned by input sources. (default)
[2]	R/W	ENQKHS	Set 0: normal operation (default) (HMeet = 64, 96 lines, hsync_dlt32 = hsync_dlt*32) Set 1: (HMeet = 4, 8 lines, hsync_dlt32 = hsync_dlt*4)

Bit	Access	Symbol	Description
[1]	R/W	ITLCPRO	Set 1 for interlaced video (default) Set 0 for non-interlaced video
[0]	R/W	ENSHDW	0: (default)

3.1.15 Source Select Register

Address Offset: 31h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	
[4]	R/W	INP_SRC_SEL	1: select digital ITU656 input 0: select analog input
[3:0]	R/W	RESERVED	

3.1.16 Interrupt Status Register

Address Offset: 32h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R	ITLCFLM	Indicates incoming video signal is interlaced
[5:0]	R/W	INTSTS	[5]: lead vsync [4]: time out [3]: hs_time_ch [2]: vs_time_ch [1]: hs_missing [0]: vs_missing

3.1.17 Interrupt Mask Register

Address Offset: 33h Access: Read/Write
Default Value: FFh Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5:0]	R/W	INTMASK	

3.1.18 Lower 8-bit Timer Counter Register

Address Offset: 35h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	TM_1MS_L [7:0]	Lower byte of the number of XCLK's in 1ms.

3.1.19 Upper 8-bit Timer Counter Register

Address Offset: 36h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	TM_1MS_H [15:8]	Higher byte of the number of XCLK's in 1ms.

3.1.20 VSYNC Missing Counter Register

Address Offset: 37h Access: Read/Write

Default Value: 40h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_MISS_CNT	

3.1.21 Lower 8-bit HSYNC Missing Counter Register

Address Offset: 38h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_MISS_CNT_L[7:0]	

3.1.22 Upper 8-bit HSYNC Missing Counter Register

Address Offset: 39h Access: Read/Write
 Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_MISS_CNT_L[15:8]	

3.1.23 VSYNC Delta Difference Result Register

Address Offset: 3Ah Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VSYNC_DLT[7:0]	

3.1.24 HSYNC Delta Difference Result Register

Address Offset: 3Bh Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HSYNC_DLT[7:0]	

3.1.25 Input Sync Signal Detection Register

Address Offset: 3Fh Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	HSTLSPVS	1:use trailing edge of hsync to sample 0:use leading edge of hsync to sample
[6]	R/W	AUTOVSD6	When the edges of vsync and hsync are too close, input detection circuit can delay vsync 6 cycle of XCLK to avoid unstable detection 1:Automatically delay 6 cycles of XCLK if CFSEEDGE is true. 0:Dealy 6 cycles of XCLK if FCVSD6 is true
[5]	R/W	FCVSD6	AUTOVSD6 FCSVSD6T 1 x Automatically delay VSync 6 XCLK if CFSEEDGE is true 0 1 Force to delay VSync 6 XCLK 0 0 No Vsync Dealy
[4]	R	CFSEEDGE	VS and HS edges are to close.
[3:2]	R/W	RESERVED	

[1]	R/W	VsHs_Sync_Edge	1: leading edge of Vsi 0: falling edge of Hsi
[0]	R/W	VsHS_Sync_En	1:leading edge of Vsi starts at leading edge of Hsi 0:leading edge of Vsi starts at mid of Hsi

3.1.26 Left Border Cropping

Address Offset: 40h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5:0]	R/W	CROP_LEFTB	Remove noisy pixels appearing on left border. 1LSB =1 pixel

3.1.27 VSYNC Timing Measurement Register

Address Offset: 50h Access: **Read Only**
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R/W	HSPMD	Register 0x5c and 0x5d can be HS pulse width or hsync period 1:Period in # of pixel clock. 0:Hsync pulse width in # of pixel clock.
[5]	R	DONE_FRMXCLKCNT	When EN_FRAMEXCLKCNT is enabled, a whole frame time can be obtained through XCLK counting. See registers 0x51, 0x52 and 0x53. After this bit read back as 1, then clear EN_FRAMEXCLKCNT first before reading 0x51~0x53 values.
[4]	R/W	EN_FRAMEXCLKCNT	When input VSync changes, enable this bit to start measurement on VSync using XCLK.
[3:0]	R/W	RESERVED	

3.1.28 VSYNC Measurement Counter L Register

Address Offset: 51h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FRMXCLK_SUM[7:0]	

3.1.29 VSYNC Measurement Counter M Register

Address Offset: 52h Access: **Read Only**
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FRMXCLK_SUM[15:8]	

3.1.30 VSYNC Measurement Counter H Register

Address Offset: 53h Access: **Read Only**
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
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[7:0]	R/W	FRMXCLK_SUM[23:16]	
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3.1.31 Hsize

Address Offset: 54h Access: **Read Only**
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	HSIZE[7:0]	

3.1.32 Hsize

Address Offset: 55h Access: **Read Only**
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R	HSIZE[11:8]	

3.1.33 Vsize

Address Offset: 56h Access: **Read Only**
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	VSIZE[7:0]	

3.1.34 Vsize

Address Offset: 57h Access: **Read Only**
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R	VSIZE[11:8]	

3.1.35 HSYNC Period LSB Register

Address Offset: 58h Access: **Read Only**
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	HS_PERIOD[7:0]	HSYNC period counted by XCLK

3.1.36 HSYNC Period MSB Register

Address Offset: 59h Access: **Read Only**
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	HS_PERIOD[15:8]	HSYNC period counted by XCLK

3.1.37 VSYNC Period LSB Register

Address Offset: 5Ah Access: **Read Only**
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	VS_PERIOD[7:0]	VSYNC period counted by input HSYNC

3.1.38 VSYNC Period MSB Register

Address Offset: 5Bh
Default Value: 00h

Access: **Read Only**
Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R	VS_PERIOD[11:8]	VSYNC period counted by input HSYNC

3.1.39 HSYNC Pulse Width LSB Register

Address Offset: 5Ch
Default Value: 00h

Access: **Read Only**
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	HS_WIDTH[7:0]	HSYNC pulse width or period counted by dot clock See HSPMD for detail. Note: dot clock speed is in 1-pixel-per-clock mode

3.1.40 HSYNC Pulse Width MSB Register

Address Offset: 5Dh
Default Value: 00h

Access: **Read Only**
Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R	RESERVED	
[3:0]	R	HS_WIDTH[11:8]	HSYNC pulse width or period counted by dot clock

3.1.41 VSYNC Pulse Width LSB Register

Address Offset: 5Eh
Default Value: 00h

Access: **Read Only**
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	VS_WIDTH[7:0]	VSYNC pulse width counted by input HSYNC

3.1.42 VSYNC Pulse Width MSB Register

Address Offset: 5Fh
Default Value: 00h

Access: **Read Only**
Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R	RESERVED	
[3:0]	R	VS_WIDTH[11:8]	VSYNC pulse width counted by input HSYNC

3.2 Picture Enhancement Register Set

3.2.1 Bandwidth of Digital Color Transient Improvement

Address Offset: 60h Access:
Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	DCTI_ADV	advanced DCTI 0: disable 1: enable (default)
[6:4]		RESERVED	
[3:2]	R/W	DCTI_BW_1	DCTI operation width 1 00: level 0 (default) 01: level 1 10: level 2 11: level 3
[1:0]	R/W	DCTI_BW_0	DCTI operation width 0 00: level 0 (default) 01: level 1 10: level 2 11: level 3

3.2.2 Gain and Coring of DCTI 0

Address Offset: 65h Access:
Default Value: 08h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	DCTI_GAIN_0	
[4:0]	R/W	DCTI_CO_0	

3.2.3 Gain and Coring of DCTI_1

Address Offset: 66h Access:
Default Value: 08h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	DCTI_GAIN_1	
[4:0]	R/W	DCTI_CO_1	

3.2.4 Cb/Cr Delay control

Address Offset: 67h Access:
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]		RESERVED	
[3:2]	R/W	U_delay	Cb signal delay control. 00: no delay (default) 01: 1 pixel delay 10: 2 pixel delay 11: 3 pixel delay

[1:0]	R/W	V_delay	Cr signal delay control. 00: no delay (default) 01: 1 pixel delay 10: 2 pixel delay 11: 3 pixel delay
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3.2.5 Contrast Adjust

Address Offset: 68h Access:
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	LumaCON	

3.2.6 Brightness Adjust

Address Offset: 69h Access:
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	LumaBRI	

3.2.7 Hue Sin Adjust

Address Offset: 6Ah Access:
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HueSin	

3.2.8 Hue Cos Adjust

Address Offset: 6Bh Access:
Default Value: 7Fh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HueCos	

3.2.9 Chroma Saturation Adjust

Address Offset: 6Ch Access:
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ChromSat	

3.3 Scaling Register Set

3.3.1 Scaling General Control Register

Address Offset: 70h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	InpClk_Phase	It might exist setup or hold time violation between ADC and input capture block. Usually, a 4-step delay unit can be applied to move pixel clock up to 4 steps to avoid timing violation.
[5]	R/W	Inv_VideoF	Inv_VideoF: Reverse input odd field control for intrafield scaling, only take action when ITLCPRO set to 1.
[4]	R/W	Dclki_is_Faster	Software need to turn this bit on when the freq of input pixel clock is higher than output pixel clock.
[3:0]		RESERVED	

3.3.2 Scaling Coefficient Data Port Register

Address Offset: 71h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Coef_Data_Port	

3.3.3 Horizontal Scale Step LSB Register

Address Offset: 72h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_Scale_Step [7:0]	

3.3.4 Horizontal Scale Step MSB Register

Address Offset: 73h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_Scale_Step [15:8]	

3.3.5 Vertical Scale Step LSB Register

Address Offset: 74h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_Scale_Step [7:0]	

3.3.6 Vertical Scale Step MSB Register

Address Offset: 75h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_Scale_Step [15:8]	

3.3.7 Horizontal Aspect Ratio Register

Address Offset: 76h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HASPR[7:0]	

3.3.8 Horizontal Aspect Ratio Register

Address Offset: 77h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	HASPEN	Aspect Ratio Enable
[6]	R/W	HASP_C_ELG	Center Enlarge
[5:4]		RESERVED	
[3:0]	R/W	HASPR[11:8]	Aspect Ratio [11:8]

3.3.9 Input Vsync Leading Edge to DE Time Counter 1/3 Register

Address Offset: 81h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	TVIBLK[7:0]	Timing counter can measure the time interval between leading edge of input vsync and first valid input pixel. This time interval is TVIBLK * (1/XCLK)

3.3.10 Input Vsync Leading Edge to DE Time Counter 2/3 Register

Address Offset: 82h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	TVIBLK [15:8]	

3.3.11 Input Vsync Leading Edge to DE Time Counter 3/3 Register

Address Offset: 83h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]		RESERVED	
[1:0]	R/W	TVIBLK[17:16]	

3.3.12 Line Buffer Configuration LSB Register

Address Offset: 84h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	LBPRFL[7:0]	LBPRFL can cause a time delay in XCLK count between the leading edge of input Vsync and leading edge of output Vsync.

3.3.13 Line Buffer Configuration MSB Register

Address Offset: 85h Access: Read/Write
 Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
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Bit	Access	Symbol	Description
[7:0]	R/W	LBPRFL[15:8]	

3.3.14 Output Vsync Front Porch Remapping Register

Address Offset: 87h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VSFPRMP	Output HSync remap amount in vertical front porch period.

3.3.15 Left Display Border Configuration Register

Address Offset: 88h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HLDSPLB[7:0]	When Output pixel's index is less than HRDSPLB, output pixel value is assigned as left display border {FMCLRRDE, FMCLRGRN, FMCLRBLU}

3.3.16 Left Display Border Configuration Register

Address Offset: 89h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	HDSPLB_INV	Horizontal border is on if HDSPLB_INV is set as follows 1: HLDSPLB < Horizontal border < HRDSPLB 0: Horizontal border < HLDSPLB or HRDSPLB < Horizontal border
[6]	R/w	VDSPLB_INV	Vertical border is on if VDSPLB_INV is set as follows 1: VTDSPLB < < VBDSPLB 0: Vertical border < VTDSPLB or VBDSPLB < Vertical border
[5]	R/W	HDSPLB_STY	Border style 1: mesh 0: solid
[4]	R/W	VDSPLB_STY	Border style 1: mesh 0: solid
[3]		RESERVED	
[2:0]	R/W	HLDSPLB[10:8]	

3.3.17 Right Display Border Configuration LSB Register

Address Offset: 8Ah Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HRDSPLB[7:0]	When Output pixel's index is greater than HRDSPLB, output pixel value is assigned as right display border {FMCLRRDE, FMCLRGRN, FMCLRBLU}

3.3.18 Right Display Border Configuration MSB Register

Address Offset: 8Bh Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
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Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[2:0]	R/W	HRDSPLB[10:8]	

3.3.19 Top Display Border Configuration LSB Register

Address Offset: 8Ch Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VTDSPLB[7:0]	

3.3.20 Top Display Border Configuration MSB Register

Address Offset: 8Dh Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	HDSPLB_GRID[1:0]	H grip precision, 00b: 1 pixel 01b: 4 pixels 10b: 16 pixels 11b: 32 pixels
[5:4]	R/W	VDSPLB_GRID[1:0]	V grip precision 00b: 1 line 01b: 4 lines 10b: 16 lines 11b: 32 lines
[3:2]		RESERVED	
[1:0]	R/W	VTDSPLB[9:8]	

3.3.21 Bottom Display Border Configuration LSB Register

Address Offset: 8Eh Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VBDSPLB[7:0]	

3.3.22 Bottom Display Border Configuration MSB Register

Address Offset: 8Fh Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[1:0]	R/W	VBDSPLB[9:8]	

3.3.23 Color Space Converter Register Set

3.3.24 Image Function Control Register

Address Offset: 90h Access: Read/Write
Default Value: 04h Size: 8 bits

	Access	Symbol	Description										
[7:6]	R/W	GATS[1:0]	Gamma Table Select. Default=2'b00. <table><tr><th>GATS[1:0]</th><th>Polarity</th></tr><tr><td>2'b11</td><td>Gamma Table R</td></tr><tr><td>2'b10</td><td>Gamma Table G</td></tr><tr><td>2'b01</td><td>Gamma Table B</td></tr><tr><td>2'b00</td><td>All 3</td></tr></table>	GATS[1:0]	Polarity	2'b11	Gamma Table R	2'b10	Gamma Table G	2'b01	Gamma Table B	2'b00	All 3
GATS[1:0]	Polarity												
2'b11	Gamma Table R												
2'b10	Gamma Table G												
2'b01	Gamma Table B												
2'b00	All 3												
[5]		RESERVED											
[4]		RESERVED											
[3]		RESERVED											
[2]	R/W	EN_CSC	Enable CSC										
[1]	R/W	EN_GAMMA	Enable Gamma.										
[0]	R/W	EN_DITHER	Enable Dithering.										

3.3.25 Built-in Pattern Generator Control Register

Address Offset: 91h Access: Read/Write
Default Value: 0Ch Size: 8 bits

	Access	Symbol	Description										
[7]	R/W	EFMCLR	Enable Frame background color Turn on this bit may disable Scaler's color and show user-defined color on LCD panel. See 0x9E, 0x9E and 0x9F for user-defined color.										
[6]	R/W	ESLDSW	This bit may enable pattern generator shows 9 patterns sequentially. <table><tr><th>EFMCLR, ESLDSW</th><th>Output</th></tr><tr><td>2'b00</td><td>Normal Color</td></tr><tr><td>2'b01</td><td>Normal Color</td></tr><tr><td>2'b10</td><td>Still pattern</td></tr><tr><td>2'b11</td><td>Motion patterns</td></tr></table>	EFMCLR, ESLDSW	Output	2'b00	Normal Color	2'b01	Normal Color	2'b10	Still pattern	2'b11	Motion patterns
EFMCLR, ESLDSW	Output												
2'b00	Normal Color												
2'b01	Normal Color												
2'b10	Still pattern												
2'b11	Motion patterns												
[5]	R/W	EVBAR	????										
[4]	R/W	PLBIT	1: indicate 8-bit patterns 0:indicate 6-bit patterns										
[3]		RESERVED											
[2:0]	R/W	PTN	Show nth pattern on LCD panel when EFMCLR is enabled When Both EFMCLR and ESLDSW are enabled, pattern generator may show 0, 1,2 ...up to PTNth. There are 12 parrerns we can show on LCD panel.										

3.3.26 GAMMA Table Address Port Register

Address Offset: 93h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	GAMMA_ADR	Gamma coefficient table address. The Index range is 00h~20h

3.3.27 GAMMA Table Write Data Port Register

Address Offset: 94h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	GAMMA_WR_D	Gamma coefficient write data port.

3.3.28 Black Level Expansion Threshold

Address Offset: 95h Access: Read/Write
 Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BLE_TH	

3.3.29 VIP Black level Expansion Gain / Offset Control Register

Address Offset: 96h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	BLE_GAIN	
[3:2]		RESERVED	
[1:0]	R/W	BLE_OFFSET	

3.3.30 Pattern Color Gradient & Dithering Mode Register

Address Offset: 9Ch Access: Read/Write
 Default Value: 00h Size: 8 bits

	Access	Symbol	Description										
[7:4]	R/W	CLRGRDT[3:0]	When both FMSW and EFMCLR are enabled, CLRGRDT may set color gradient at pattern 2, 3, 4, 5										
[3:2]		RESERVED											
[1:0]	R/W	DITHER_MD	Dithering mode. It is enabled by register 90h. <table><tr><th>DITHER_MD</th><th>Output</th></tr><tr><td>2'b00</td><td>4-bit output</td></tr><tr><td>2'b01</td><td>5-bit output</td></tr><tr><td>2'b10</td><td>6-bit output</td></tr><tr><td>2'b11</td><td>7-bit output</td></tr></table>	DITHER_MD	Output	2'b00	4-bit output	2'b01	5-bit output	2'b10	6-bit output	2'b11	7-bit output
DITHER_MD	Output												
2'b00	4-bit output												
2'b01	5-bit output												
2'b10	6-bit output												
2'b11	7-bit output												

3.3.31 Frame Color Red Configuration Register

Address Offset: 9Dh Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FMCLRRDE	8 bits of red color depth for frame color.

3.3.32 Frame Color Green Configuration Register

Address Offset: 9Eh Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FMCLGRGN	8 bits of green color depth for frame color.

3.3.33 Frame Color Blue Configuration Register

Address Offset: 9Fh

Access: Read/Write

Default Value: 00h

Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FMCLRBLU	8 bits of blue color depth for frame color.

3.4 OSD Register Set

(For detail OSD description, please refer to 2 Theory of Operation--OSD section.)

3.4.1 OSD Configuration Index Port Register

Address Offset: A0h Access: Write Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	W	OSD_CFG_INDEX	OSD Configuration Address Port

3.4.2 OSD Configuration Data Port Register

Address Offset: A1h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD_CFG_DATA	OSD Configuration Data Port

3.4.3 OSD RAM Address Port LSB Register

Address Offset: A2h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD_RAM_AL	OSD RAM Address Port LSB

3.4.4 OSD RAM Address Port MSB Register

Address Offset: A3h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD_RAM_AH	OSD RAM Address Port MSB

3.4.5 OSD RAM Data Port Register

Address Offset: A4h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD_RAM_D	OSD RAM Data Port

3.5 LCD Output Control Register Set

3.5.1 Display Window Horizontal Start Register

Address Offset: B0h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DWHS_L[7:0]	Horizontal back porch.

3.5.2 Display Window Vertical Start Register

Address Offset: B2h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DWVS[7:0]	Vertical back porch

3.5.3 Display Window Horizontal Width LSB Register

Address Offset: B4h Access: Read/Write
Default Value: E0h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DWHSZ[7:0]	Horizontal Active.

3.5.4 Display Window Horizontal Width MSB Register

Address Offset: B5h Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[2:0]	R/W	DWHSZ[10:0]	Horizontal Active.

3.5.5 Display Window Vertical Width LSB Register

Address Offset: B6h Access: Read/Write
Default Value: EAh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DWVSZ[7:0]	Vertical Active.

3.5.6 Display Window Vertical Width MSB Register

Address Offset: B7h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[1:0]	R/W	DWVSZ[9:8]	

3.5.7 Display Panel Horizontal Total Dots per Scan Line LSB Register

Address Offset: B8h Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PH_TOT[7:0]	Output horizontal total dots

3.5.8 Display Panel Horizontal Total Dots per Scan Line MSB Register

Address Offset: B9h Access: Read/Write
 Default Value: 03h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[2:0]	R/W	PH_TOT[10:8]	

3.5.9 Display Panel Vertical Total Lines per Frame LSB Register

Address Offset: BAh Access: Read/Write
 Default Value: 58h Size: 8 bits

	Access		Description
[7:0]	R/W	PV_TOT[7:0]	Output vertical total lines

3.5.10 Display Panel Vertical Total Lines per Frame MSB Register

Address Offset: BBh Access: Read/Write
 Default Value: 02h Size: 8 bits

Bit		Symbol	Description
[7:2]	R/W	RESERVED	
[1:0]	R/W	PV_TOT[9:8]	

3.5.11 Display Panel HSYNC Width Register

Address Offset: BCh Access: Read/Write
 Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PH_PW[7:0]	

3.5.12 Display Panel VSYNC Width Register

Address Offset: BEh Access: Read/Write
 Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]		RESERVED	
[4:0]	R/W	PV_PW[4:0]	

3.5.13 Panel Output Signal Control 1 Register

Address Offset: C0h Access: Read/Write
 Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description						
[7:3]	R/W	RESERVED							
[2]	R/W	POUT_CTL1[2]	PHSYNC Polarity. Default=0. <table><tr><th>POUT_CTL1[2]</th><th>Polarity</th></tr><tr><td>0</td><td>ACTIVE LOW</td></tr><tr><td>1</td><td>ACTIVE HIGH</td></tr></table>	POUT_CTL1[2]	Polarity	0	ACTIVE LOW	1	ACTIVE HIGH
POUT_CTL1[2]	Polarity								
0	ACTIVE LOW								
1	ACTIVE HIGH								
[1]	R/W	POUT_CTL1[1]	PVSYNC Polarity. Default=0. <table><tr><th>POUT_CTL1[1]</th><th>Polarity</th></tr><tr><td>0</td><td>ACTIVE LOW</td></tr><tr><td>1</td><td>ACTIVE HIGH</td></tr></table>	POUT_CTL1[1]	Polarity	0	ACTIVE LOW	1	ACTIVE HIGH
POUT_CTL1[1]	Polarity								
0	ACTIVE LOW								
1	ACTIVE HIGH								

Bit	Access	Symbol	Description	
[0]	R/W	POUT_CTL1[0]	PDE polarity. Default=0.	
			POUT_CTL1[0]	Polarity
			0	ACTIVE LOW
			1	ACTIVE HIGH

3.5.14 Panel Output Signal Control 3 Register

Address Offset: C1h Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol							
[7:4]	R/W	RESERVED							
[3]	R/W	DCLK_INV	DCLK Polarity. Default=0. <table><tr><td>DCLK_INV</td><td>Mode</td></tr><tr><td>0</td><td>Normal</td></tr><tr><td>1</td><td>Inverted</td></tr></table>	DCLK_INV	Mode	0	Normal	1	Inverted
DCLK_INV	Mode								
0	Normal								
1	Inverted								
[2]	R/W	LVDS_MD	ODCK Internal Delay. Default=0. <table><tr><td>LVDS_MD</td><td>Mode</td></tr><tr><td>0</td><td>Natinal standard</td></tr><tr><td>1</td><td>Korean/Non-standard</td></tr></table>	LVDS_MD	Mode	0	Natinal standard	1	Korean/Non-standard
LVDS_MD	Mode								
0	Natinal standard								
1	Korean/Non-standard								
[1:0]	R/W	Reserved							

3.5.15 Panel VSYNC Frame Delay Control Register

Address Offset: C2h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]		RESERVED	
[6:5]	R/W	Hso_2_Vso_Delay	
[4]	R/W	PSYNC_STR	1:Block input vsync triggering on output vsync 0: Allow input vsync to trigger output vsync
[3]	R/W	ELASTPHS	0= Short line, i.e., last hsync is less than 1.0 line 1= Long line, i.e., last hsync is greater than 1.0 line
[2]		RESREVED	
[1]	R/W	IGNORE_VSYNC	Ignore the input VSYNC. This can be used for output free run when input VSYN is not available
[0]	R/W	RESERVED	

3.5.16 Panel VSYNC Frame Delay Line Count LSB Register

Address Offset: C3h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PV_DELAY_L	

3.5.17 Panel VSYNC Frame Delay Line Count MSB Register

Address Offset: C4h Access: Read/Write

Default Value: 00h

Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	R/W	RESERVED	
[1:0]	R/W	PV_DELAY_H	Delay last stage VSync output, in the unit of output HSync leading edge.

3.5.18 Output RGB Reordering Register

Address Offset: C7h

Access: Read/Write

Default Value: 00h

Size: 8 bits

Bit	Access	Symbol	Description
[7:4]		RESERVED	
[3]	R/W	BIGENDIANE	Reverse bit [7:0] of RGB on even channel
[2:0]	R/W	RGBSWAPE	See diagram

3.5.19 Output PLL Divider 1 Register

Address Offset: C8h

Access: Read/Write

Default Value: 15h

Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	Reserved	
[6:0]	R/W	PLLDIV_F	PLL feedback divider. Default=124.

3.5.20 Output PLL Divider 2 Register

Address Offset: C9h

Access: Read/Write

Default Value: 02h

Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	Reserved	
[4:0]	R/W	PLLDIV_I	PLL Input Divider. Default=27.

3.5.21 Output PLL Divider 3 Register

Address Offset: CAh

Access: Read/Write

Default Value: 03h

Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	PLLMX	PLL MUX Function Select
			PLLMX
			Mode
			2'b00
			2'b01
			Bypass PLL
[5]	R/W	PLLPD	1: Display PLL power down
			0: Display PLL power on
[4]	R/W	Reserved	
[3:2]	R/W	PLL_OUT_SEL	PLL additional divider 0: no divider 1: divided by 2 2: divided by 4 3: divided by 8
[1:0]	R/W	PLLDIV_O	PLL Output Divider. Default=1. $\text{output_freq} = 27\text{Mhz} * (F + 2) / (I + 2) / (2^{(O+1)})$

3.5.22 Horizontal Main Display Start

Address Offset: D8h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HMDISP_STR[7:0]	

3.5.23 Vertical Main Display Start

Address Offset: DAh Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VMDISP_STR	

3.5.24 Horizontal Main Display Size

Address Offset: DCh Access: Read/Write
 Default Value: E0h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HMDISP_SIZE[7:0]	

3.5.25 Horizontal Main Display Size

Address Offset: DDh Access: Read/Write
 Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[2:0]	R/W	HMDISP_SIZE[10:8]	

3.5.26 Vertical Main Display Size

Address Offset: DEh Access: Read/Write
 Default Value: EAh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VMDISP_SIZE[7:0]	

3.5.27 Vertical Main Display Size

Address Offset: DFh Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	R/W	RESERVED	
[1:0]	R/W	VMDISP_SIZE[9:8]	

3.5.28 Power Management Control Register

Address Offset: E0h Access: Read/Write
 Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	TPDB	I/O pad power down. Low active
[6]	R/W	RESERVED	
[5]	R/W	RESERVED	
[4]	R/W	PDC_B	Power Down Comb Video Decoder. For internal software test. Low active.

Bit	Access	Symbol	Description
[3]	R/W	LLCK1_EN	LLCK1 enable
[2]	R/W	LLCK2_EN	LLCK2 enable
[1]	R/W	LLCK3_EN	LLCK3 enable
[0]	R/W	PWDNTC	Power down TC interface. Low active

3.5.29 Output Pin Configuration

Address Offset: E1h
Default Value: 00h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	RowSTV_Sel	RowSTV_Sel
			Mode
			2'b00 Output both
			2'b01 Output both
			2'b10 Output STV1
			2'b11 Output STV2
[5:4]	R/W	ColSTH_Sel	ColSTH_Sel
			Mode
			2'b00 Output both
			2'b01 Output both
			2'b10 Output STH1
			2'b11 Output STH2
[3]	R/W	UD_SEL	
[2]	R/W	LR_SEL	
[1:0]	R/W	RESERVED	

3.5.30 DAC Power Management

Address Offset: E3h
Default Value: 00h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3]	R/W	SL	1: power down 3 channels 0: power on 3 channels
[2]	R/W	SLR	1: power down R channel 0: power on R channel
[1]	R/W	SLG	1: power down G channel 0: power on G channel
[0]	R/W	SLB	1: power down B channel 0: power on B channel

3.5.31 PWM_3 General Control Register

Address Offset: E6h
Default Value: 07h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	
[4]	R/W	VPWME_3	Enable Volume PWM_3
[3]	R/W	RESERVED	

[2:0]	R/W	VPWM_FREQ_SEL_3	This register allow base clock has 7 types of clock freqs divided from XCLK . 000 = XCLK/2 ³ 001 = XCLK/2 ⁵ 010 = XCLK/2 ⁷ 011 =XCLK/2 ⁹ 100 =XCLK/2 ¹¹ 101= XCLK/2 ¹³ 110=XCLK/2 ¹⁵ 111=XCLK/2 ¹⁷
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3.5.32 PWM_3 Active High Time Counter Register

Address Offset: E7h Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VPWM_HIGH_3	This register may allow volume PWM high time counted by base clock The based clock is divide from XCLK , see 0xE6[2:0]

3.5.33 PWM_1 General Control Register

Address Offset: E8h Access: Read/Write
Default Value: 07h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	
[4]	R/W	VPWME_1	Enable Volume PWM
[3]	R/W	RESERVED	
[2:0]	R/W	VPWM_FREQ_SEL_1	This register allow base clock has 7 types of clock freqs divided from XCLK . 000 = XCLK/2 ³ 001 = XCLK/2 ⁵ 010 = XCLK/2 ⁷ 011 =XCLK/2 ⁹ 100 =XCLK/2 ¹¹ 101= XCLK/2 ¹³ 110=XCLK/2 ¹⁵ 111=XCLK/2 ¹⁷

3.5.34 PWM_1 Active High Time Counter Register

Address Offset: E9h Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VPWM_HIGH_1	This register may allow volume PWM high time counted by base clock The based clock is divide from XCLK , see 0xE8[2:0]

3.5.35 PWM_2 General Control Register

Address Offset: EAh Access: Read/Write
Default Value: 07h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	

[4]	R/W	VPWME_3	Enable Volume PWM
[3]	R/W	RESERVED	
[2:0]	R/W	VPWM_FREQ_SEL_2	This register allow base clock has 7 types of clock freqs divided from XCLK . 000 = XCLK/2^3 001 = XCLK/2^5 010 = XCLK/2^7 011 =XCLK/2^9 100 =XCLK/2^11 101= XCLK/2^13 110=XCLK/2^15 111=XCLK/2^17

3.5.36 PWM_2 Active High Time Counter Register

Address Offset: EBh Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VPWM_HIGH_2	This register may allow volume PWM high time counted by base clock The based clock is divide from XCLK , see 0xEA[2:0]

3.5.37 GPIO Output Control Register

Address Offset: ECh Access: Read/Write
Default Value: C0h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	GPIO_OUT	GPIO[3:0] output data
[3:0]	R/W	GPIO_OE[3:0]	GPIO[3:0] output enable 0: input 1: output

3.5.38 GPIO Input/Interrupt Status Register

Address Offset: EDh Access: Read Only
Default Value: - Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	GPIO_INPUT[3:0]	GPIO[3:0] input data
[3:0]	R/W	GPIO_INT[3:0]	GPIO[3:0] interrupt status/mask. Write 1 to clear.

3.5.39 GPIO Input Rising/Falling Edge Detect Register

Address Offset: EEh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	En_Fall_GPIO[3:0]	Enable GPIO[3:0] falling edge detection.
[3:0]	R/W	En_Rise_GPIO[3:0]	Enable GPIO[3:0] rising edge detection.

3.5.40 GPIO Input De-bounce Control Register

Address Offset: EFh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
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[7:6]	R/W	DeBounce_Sel_1	GPIO[3:2] interrupt de-bounce selection. 00: 1ms 01: 2ms 10: 4ms 11: 8ms
[5:4]	R/W	DeBounce_Sel_0	GPIO[1:0] interrupt de-bounce selection. 00: 1ms 01: 2ms 10: 4ms 11: 8ms
[3:0]	R/W	En_DeBounce[3:0]	Enable GPIO[3:0] interrupt de-bounce function.

3.5.41 Serial Bus Slave Device Address Register

Address Offset: F0h Access: Read/Write
Default Value: 40/50h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	SDADDR	default = 40 if SDA is low while reset default = 50 if SDA is high while reset
[3:0]	R/W	Reserved	

3.5.42

Address Offset: F1h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit		Symbol	Description						
[7:3]	R/W	RESERVED							
[2]	R/W	I2CATINCADR	Enable 2-wire serial bus automatic address increment in multiple R/W Access mode. Default=1'b1. <table><tr><th>Mode</th><th>INC</th></tr><tr><td>1'b0</td><td>STOP INC</td></tr><tr><td>1'b1</td><td>Auto INC</td></tr></table>	Mode	INC	1'b0	STOP INC	1'b1	Auto INC
Mode	INC								
1'b0	STOP INC								
1'b1	Auto INC								
[1:0]	R/W	RESERVED							

3.5.43 Vendor ID 1 Register

Address Offset: F3h Access: **Read Only**
Default Value: 54h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	VID_L	Reading this register obtains ASCII code "T". Hex value is 54h

3.5.44 Vendor ID 2 Register

Address Offset: F4h Access: **Read Only**
Default Value: 57h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	VID_H	Reading this register obtains ASCII code "W".

3.5.45

Address Offset: F5h Access: **Read Only**
Default Value: C2h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	DID	This field puts a part number in Hex "C2".

3.5.46 Revision ID Register

Address Offset: F6h Access: **Read Only**
 Default Value: A1h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R	RID	This field puts a revision number in Hex "A1".

3.5.47 Debug Mode

Address Offset: FEh Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]		RESERVED	
[2]	R/W	BYPS_CLAMP	
[1]	R/W	BYPS_VD	
[0]	R/W	BYPS_ADC	

3.5.48 Page Select Register

Address Offset: FFh Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[2:0]	R/W	PAGE[2:0]	

Serial Bus Register Set Page 1

3.6 TCON Register Set

3.6.1 Timing Controller (TCON) Control Register

Address Offset: 20h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]		RESERVED	
[6]		RESERVED	
[5]	R/W	GTOE	Enable gate driver output Mode 0 Type 1 Shutdown output Enable
[4]		RESERVED	
[3]		RESERVED	
[2]		RESERVED	
[1]	R/W	Q1HPL	Q1H polarity
[0]	R/W	PNINV	Enable line-inverted function.

3.6.2 Timing Protocol & Polarity Control Register

Address Offset: 21h Access: Read/Write
Default Value: 7Fh Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R/W	GTOEPL	This bit may control GOE polarity Mode 0 Type 1 Low-active Highactive
[5]	R/W	STVPL	Row Driver start pulse polarity Mode 0 Type 1 Negative Positive
[4]	R/W	CLKVPL	Data Inversion Polarity Mode 0 Type 1 Negative Positive
[3]	R/W	INVOPL	Data Inversion Polarity Mode 0 Type 1 Negative Positive
[2]	R/W	POLPL	Column Driver POL inversion polarity Mode 0 Type 1 Negative Positive

[1]	R/W	LPPL	Column Driver Latch Pulse polarity Mode 0 1 Type Negative Positive
[0]	R/W	STHPL	Column Driver Start Pulse polarity Mode 0 1 Type Negative Positive

3.6.3 Column Driver Latch Pulse Placement LSB Register

Address Offset: 22h Access: Read/Write
Default Value: 03h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CDLPPLM[7:0]	This register allows LP to place between 2 DE pulses counted by LLCK dot clock The reference point is the rising edge of DE.

3.6.4 Column Driver Latch Pulse Placement MSB Register

Address Offset: 23h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	CDLPPLM[11:8]	This register allows LP to place between 2 DE pulses counted by LLCK dot clock The reference point is the rising edge of DE.

3.6.5 Column Driver Latch Pulse Duration Control Register

Address Offset: 24h Access: Read/Write
Default Value: 21h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CDLPDU[7:0]	This register allows LP duration programmable. counted by LLCK dot clock.

3.6.6 POL Placement LSB Register

Address Offset: 25h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	POLPLM[7:0]	The reference point is the leading edge of DE.

3.6.7 POL Placement MSB Register

Address Offset: 26h Access: Read/Write
Default Value: 00h Size: 8 bits



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3.6.8 CLKV Placement LSB Register

Address Offset: 27h Access: Read/Write

Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CLKVPLM[7:0]	The reference point is the leading edge of DE

3.6.9 CLKV Placement MSB Register

Address Offset: 28h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	CLKVPLM[11:8]	The reference point is the leading edge of DE

3.6.10 CLKV Duration LSB Register

Address Offset: 29h Access: Read/Write
 Default Value: 0Fh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CLKVDU[7:0]	The reference point is leading edge of DE

3.6.11 CLKV Duration MSB Register

Address Offset: 2Ah Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	CLKVDU[11:8]	The reference point is the leading edge of DE

3.6.12 STH Position Placement Register

Address Offset: 2Bh Access: Read/Write
 Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[2:0]	R/W	STHPLM[2:0]	STH timing related to HDE. -2 to 5 CLKHs

3.6.13 Reserved

Address Offset: 2Ch Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	

3.6.14 Gate Driver Predriving

Address Offset: 2Dh Access: Read/Write
 Default Value: 03h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	GDPredDu	

3.6.15 Row Driver Configuration Register

Address Offset: 30h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:1]	R/W	RESERVED	
[0]	R/W	ESTVOFFSET	

3.6.16 Gate Driver OE Pulse Position Placement LSB Register

Address Offset: 31h Access: Read/Write
 Default Value: 0Fh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	GOEPL[7:0]	

3.6.17 Gate Driver OE Pulse Position Placement MSB Register

Address Offset: 32h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	GOEPL[11:8]	

3.6.18 Gate Driver OE Pulse Duration LSB Register

Address Offset: 33h Access: Read/Write
 Default Value: 0Fh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	GOEDU[7:0]	

3.6.19 Gate Driver OE Pulse Duration MSB Register

Address Offset: 34h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	GOEDU[11:8]	

3.6.20 STV Offset Register

Address Offset: 35h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	STVOFF[7:0]	

3.7 ITU - 656 Decoder Register Set

3.7.1 ITU-656 Decoder HS Delay

Address Offset: D0h Access: Read/Write
Default Value: 30h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HS_DELAY656[7:0]	Unit: Cycles of Half VCLK

3.7.2 ITU-656 Decoder HS Delay

Address Offset: D1h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	HS_DELAY656[11:8]	

3.7.3 ITU-656 Decoder HS Pulse Width

Address Offset: D2h Access: Read/Write
Default Value: 20h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HS_WIDTH656[7:0]	Unit: Cycles of Half VCLK

3.7.4 ITU-656 Decoder VS Delay

Address Offset: D3h Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VS_DELAY656[7:0]	Unit: HS

3.7.5 ITU-656 Decoder VS Pulse Width

Address Offset: D4h Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	VS_WIDTH656[3:0]	Unit: HS

3.7.6 ITU-656 Decoder HDE Start

Address Offset: D5h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HSTART656[7:0]	Unit: Pixel

3.7.7 ITU-656 Decoder HDE Start

Address Offset: D6h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	

[3:0]	R/W	HSTART656[11:8]	Unit: Pixel
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3.7.8 ITU-656 Decoder HDE Size

Address Offset: D7h Access: Read/Write
 Default Value: D0h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HSIZE656[7:0]	Unit: Pixel

3.7.9 ITU-656 Decoder HDE Size

Address Offset: D8h Access: Read/Write
 Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/w	HSIZE656[11:8]	Unit: Pixel

3.7.10 ITU-656 Decoder Odd Field VDE Start

Address Offset: D9h Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OVSTART656[7:0]	Unit: HS

3.7.11 ITU-656 Decoder Odd/Even Field VDE Start

Address Offset: DAh Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	EVPluse1	Even Filed VDE Start 1: EVSTART656=OVSTART + 1 0: EVSTART656=OVSTART
[6:4]	R/W	RESERVED	
[3:0]	R/W	OVSTART656[11:8]	Odd Filed VDE Start Unit: HS

3.7.12 ITU-656 Decoder VDE Size

Address Offset: DBh Access: Read/Write
 Default Value: F0h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VSIZE656[7:0]	Unit: HS

3.7.13 ITU-656 Decoder VDE Size

Address Offset: DCh Access: Read/Write
 Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	VSIZE656[11:8]	Unit: HS

3.7.14 ITU-656 Decoder VCLK Tuning

Address Offset: Deh Access: Read/Write
 Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	601_enable	0: disable (default) 1: enable
[6]		RESERVED	
[5]	R/W	LODD_INV	
[4]	R/W	LODD_VSYNC	
[3]	R/W	LHREF_INV	
[2]	R/W	LFIEDLD_LHREF	
[1]	R/W	VCLK_INV	
[0]	R/W	VCLK_DLY	Unit: 2ns

3.7.15 ITU-656 Decoder Format Control

Address Offset: DFh
Default Value: 4Ch

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R/W	ODDF_INV	Filed flag indicator 0: 1 st field =0, 2 nd field=1 1: 1 st filed =1, 2 nd field=0
[5]		RESERVED	
[4]	R/W	VDT_IN_SEL	656/601 port selection. 0: VDT set (default) 1: VDT1 set
[3:2]		RESERVED	
[1]	R/W	SIZE_DET	Read back Size of HDE and VDE 1:Enable 0:Disable
[0]	R/W	URBK_DET	1:Keep previous detection 0:Update current detection

3.8 Y/C Separation and Chroma Decoder Register Set

Serial Bus Register Set Page 2

3.8.1 Video Source Selection of Comb Filter

Address Offset: 00h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]		RESERVED	
[5]	R/W	PIXEL_CNT	Pixel per scan line. 0: 858 pixels (default) 1: 864 pixels
[4]	R/W	LINE_CNT	Scan lines per frame. 0 = 525 (default) 1 = 625
[3:1]	R/W	TV_MODE	Video standard. 000 = NTSC (default) 001 = PAL (I,B,G,H,D,N) 010 = PAL (M) 011 = PAL (CN) 100 = SECAM
[0]	R/W	INPUT_MODE	Video format. 0 = composite (default) 1 = S-Video (separated Y/C)

3.8.2 Bandwidth Control

Address Offset: 01h Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]		RESERVED	
[5:4]	R/W	LUMA_FILTER	Luma notch filter bandwidth 00 = none (default) 01 = narrow 10 = medium 11 = wide
[3:2]	R/W	CHROMA_FILTER	Chroma low pass filter bandwidth 0 = narrow (default) 1 = wide 2 = extra wide 3 = extra wide
[1]	R/W	BURST_NUMBER	Burst gate width 0 = 5 sub-carrier clock cycles (default) 1 = 10 sub-carrier clock cycles
[0]	R/W	PED_ENABLE	Blank-to-black pedestal enable 0 = no pedestal sub-traction 1 = pedestal sub-traction (default)

3.8.3 Y/C AGC Enable

Address Offset: 02h Access: Read/Write
Default Value: 4fh Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	GAIN_UPDATE	Gain updating mode. 0 = per line (default) 1 = per field

[6]		REVSERVED	
[5:4]	R/W	CLAMP_MODE	DC clamping position 00 = auto (default) 01 = backporch only 10 = synctip only 11 = off
[3]	R/W	DGAIN_EN	Digital AGC enable 0 = off 1 = on (default)
[2]	R/W	RESERVED	
[1]	R/W	C_AGC_EN	Fixed chroma AGC enable. 0 = off 1 = on (default)
[0]	R/W	L_AGC_EN	Fixed luma/composite AGC enable. 0 = off 1 = on (default)

3.8.4 Comb Filtering Mode

Address Offset: 03h
Default Value: 00h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[2:0]	R/W	COMB_MODE	000 = fully adaptive comb (2-D adaptive comb) (default) 010 = 5-tap adaptive comb filter (PAL mode only) 011 = must be used for S-Video 110 = 5-tap hybrid adaptive comb filter (PAL mode only) others = reserved.

3.8.5 Luma AGC Target Value

Address Offset: 04h
Default Value: ddh

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	AGC_LEVEL	Luma AGC target value.
			Standard
			NTSC M
			NTSC J
			PAL B,D,G,H,I, COMB N, SECAM
			Programming Value
			DDh (221d) (default)
			CDh (205d)
			DCh (220d)
			DDh (221d)

3.8.6 Y/C Output Control

Address Offset: 07h
Default Value: 20h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5:4]	R/W	BLUE_SCREEN	This bit controls the blue screen mode. 00 = Disabled 01 = Enabled 10 = Auto (Default) 11 = reserved
[3:0]	R/W	YC_DELAY	The range is [-5,7]. Default = 0.

3.8.7 Luma Contrast

Address Offset: 08h
Default Value: 80h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CONTRAST	$Luma_out = Luma_in * CONTRAST$ where CONTRAST is a 1.7-bit fixed point value.

3.8.8 Luma Brightness

Address Offset: 09h Access: Read/Write
Default Value: 20h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BRIGHTNESS	$Luma_out = Luma_in + BRIGHTNESS - 32$

3.8.9 Chroma Saturation

Address Offset: 0Ah Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	SATURATION	$Chroma_out = Chroma_in * SATURATION$ where SATURATION is a 1.7-bit fixed point value

3.8.10 Chroma Hue Phase

Address Offset: 0Bh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HUE	$U_out = U_in * \cos(HUE/256*360) + V_in * \sin(HUE/256*360)$ $V_out = V_in * \cos(HUE/256*360) - U_in * \sin(HUE/256*360)$

3.8.11 Chroma AGC

Address Offset: 0Ch Access: Read/Write
Default Value: 8ah Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CHROMA_AGC	Chroma AGC target. Default = 138.

3.8.12 AGC Peak Nomial

Address Offset: 10h Access: Read/Write
Default Value: 0ah Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6:0]	R/W	AGC_PEAK	Luma peak value. Default = 10.

3.8.13 Chroma DTO Incremental 0

Address Offset: 18h Access: Read/Write
Default Value: 21h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	CHROMA_FREQ_FIX	Fixed chroma frequency. 0: disable 1: enable.
[6]		RESERVED	
[5:0]	R/W	C_FREQ[29:24]	Bits 29:24 of the 30-bit-wide chroma frequency increment.

3.8.14 Chroma DTO Incremental 1

Address Offset: 19h Access: Read/Write

Default Value: f0h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	C_FREQ[23:16]	Bits 23:16 of the 30-bit-wide chroma frequency increment.

3.8.15 Chroma DTO Incremental 2

Address Offset: 1Ah Access: Read/Write
Default Value: 7ch Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	C_FREQ[15:8]	Bits 15:8 of the 30-bit-wide chroma frequency increment.

3.8.16 Chroma DTO Incremental 3

Address Offset: 1Bh Access: Read/Write
Default Value: 0fh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	C_FREQ[7:0]	Bits 7:0 of the 30-bit-wide chroma frequency increment.

3.8.17 Active Video Horizontal Start Time

Address Offset: 2Eh Access: Read/Write
Default Value: 82h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_START	Active video horizontal start position. Default = 130.

3.8.18 Active Video Horizontal Width

Address Offset: 2Fh Access: Read/Write
Default Value: 50h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_WIDTH	Active video horizontal pixel counts. Default = 80, 640+80 = 720

3.8.19 Active Video Vertical Start

Address Offset: 30h Access: Read/Write
Default Value: 22h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_START	Active video vertical line start position. Default = 34.

3.8.20 Active Video Vertical Height

Address Offset: 31h Access: Read/Write
Default Value: 61h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_WIDTH	Active video vertical line counts. Default = 97, 384+97 = 481 half lines

3.8.21 Comb Video Status Register 1

Address Offset: 3Ah Access: Read only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
-----	--------	--------	-------------

[7:5]	R	mv_colourstripes	Macrovision color stripes detected. The number indicates the number of color stripe lines in each group
[4]	R	mv_vbi_detected	MacroVision VBI pseudo-sync pulses detection 1 = Detected 0 = Undetected
[3]	R	chromalock	Chroma PLL locked to color burst 1 = Locked 0 = Unlocked
[2]	R	vlock	Vertical lock 1 = Locked 0 = Unlocked
[1]	R	hlock	Horizontal line locked 1 = Locked 0 = Unlocked
[0]	R	no_signal	No signal detection 1 = No Signal Detected 0 = Signal Detected

3.8.22 Comb Video Status Register 2

Address Offset: 3Bh
Default Value: 00h

Access: Read only
Size: 8 bits

Bit	Access	Symbol	Description
[7:1]		RESERVED	
[0]	R	Proscan_detected	Progressive Scan Video Detected

3.8.23 Comb Video Status Register 3

Address Offset: 3Ch
Default Value: 00h

Access: Read only
Size: 8 bits

Bit	Access	Symbol	Description
[7]	R	vcr_rew	VCR Rewind Detected
[6]	R	vcr_ff	VCR Fast-Forward Detected
[5]	R	vcr_trick	VCR Trick-Mode Detected
[4]	R	vcr	VCR Detected
[3]	R	noisy	Noisy Signal Detected. This bit is set when the detected noise value (status register P2_7Fh) is greater than the value programmed into the "noise_thresh" register (P2_05h).
[2]	R	vline_625_detected	625 Scan Lines Detected
[1]	R	secam_detected	SECAM Color Mode Detected
[0]	R	pal_detected	PAL Color Mode Detected

3.8.24 Soft Reset

Address Offset: 3Fh
Default Value: 01h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:1]		RESERVED	
[0]	R/W	RESET	Soft Reset: Write 1 to reset initial values for comb filter

3.8.25 Luminance Peaking Control

Address Offset: 80h
Default Value: 04h

Access: Read/Write
Size: 8 bits

Bit	Access	Symbol	Description
[7:6]		RESERVED	

[5:4]	R/W	PEAK_RANGE	<p>Setting peak_range value</p> <p>00 1 (default)</p> <p>01 2</p> <p>10 4</p> <p>11 8</p> <p>$Y_{peak} = Y + YH * (peak_gain / peak_range)$ where Y is the luma and YH is the high frequency luma only</p>
[3:1]	R/W	PEAK_GAIN	The gain of peaking filter
[0]	R/W	PEAK_EN	<p>Luma horizontal peaking control enable.</p> <p>0 = Disabled (default)</p> <p>1 = Enabled</p>

3.8.26 Comb Filter Configuration

Address Offset: 82h

Access: Read/Write

Default Value: 42h

Size: 8 bits

Bit	Access	Symbol	Description
[7]		RESERVED	
[6]	R/W	PAL_ERR	<p>PAL error reduced.</p> <p>0: disable.</p> <p>1: enable.</p>
[5]	R/W	PAL_AUTO_EN	<p>PAL error detect enable</p> <p>0: disable.</p> <p>1: enable.</p>
[4]	R/W	COMB_PAL	<p>PAL comb filter enable.</p> <p>0: disable.</p> <p>1: enable.</p>
[3:2]		RESERVED	
[1:0]	R/W	PAL_SW_LEVEL	<p>PAL switch level.</p> <p>Default = 2.</p>

4 Electrical Characteristics

4.1 Digital I/O Pad Operation Condition

Table 4-1 Operation Condition

	Parameter	Min	Typ	Max
VDD25	Digital Core Power Supply	2.25V	2.50V	2.75V
VD33	Digital I/O Power Supply	3.0V	3.3V	3.6V
V _{IL}	Input Low Voltage	-0.3V		0.8V
V _{IH}	Input High Voltage	2.0V		5.0V
V _{T+}	Schmitt Trigger Low-to-High Threshold	1.44V	1.58V	1.71V
V _{T-}	Schmitt Trigger High-to-Low Threshold	1.09V	1.19V	1.31V
I _I	Input Leakage Current@ V _I =3.3V or 0V			±1μA
I _{OZ}	Tri-state Output Leakage Current@ V _O =3.3V or 0V			±1μA
I _{OL}	Low level Output Current@ V _{OL} =0.4V			
	2mA	2.1mA	3.4mA	4.2mA
	4mA	4.2mA	6.9mA	8.6mA
	8mA	8.4mA	13.9mA	17.2mA
	12mA	12.5mA	20.8mA	25.8mA
I _{OH}	High level Output Current@ V _{OH} =2.4V			
	2mA	3.0mA	6.2mA	10.0mA
	4mA	5.7mA	11.6mA	18.6mA
	8mA	9.5mA	19.4mA	30.9mA
	12mA	13.3mA	27.1mA	43.3mA
R _{PU}	Pull-up resistor	74KΩ	104KΩ	177KΩ
R _{PD}	Pull-down resistor	62KΩ	90KΩ	176KΩ

Note: R_{PU} and R_{PD} are always present no matter normal operation or power down mode is enabled. A typical 30~40μA false leakage current which is resulted from R_{PU} and R_{PD} when a tester forces I/O to 3.3V or 0.0 V.

4.2 DC Characteristics

(DVDD=AVDD=2.5V; AVD33R=AVD33G=AVD33B=3.3V; VREFIN=1.235V; RL=37.5ohm, CL=10pF; RSET=386ohm; Temp=75oC, unless otherwise noted)

Table 4-2 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating voltage range	AVD33R AVD33G AVD33B	3.0	3.3	3.6	V	
Operating voltage range	AVDD	2.25	2.5	2.75	V	
Operating voltage range	DVDD	2.25	2.5	2.75	V	
AVD33R supply current	IAVD33R	--	35	--	mA	SL=0, SLR=0
AVD33G supply current	IAVD33G	--	35	--	mA	SL=0, SLG=0
AVD33B supply current	IAVD33B	--	35	--	mA	SL=0, SLB=0
AVDD supply current	IAVD33	--	1	--	mA	SL=0
VDD supply current	IDVDD	--	TBD	--	mA	
Full scale current	IOFS	2.00	34.08	--	mA	Full-Scale adjust resistor. A resistor should be connected between this pin and AVS33 to control the magnitude of the full-scale video signal. $RSET(ohm)=VREFIN(V)*10.66/IOFS(A)$,where IOFS is full-scale output current.
Output voltage range	V(IO)	--	1.28	--	V	.
DAC resolution	--	--	10	--	bits	.
Integral non-linearity error	INL	--	0.5	+2	LSB	.
Differential non-linearity error	DNL	--	0.5	+1	LSB	.
Gain error	--	--	--	TBD	%	.
DAC to DAC matching	--	--	TBD	TBD	%	.

4.3 AC Characteristics

(DVDD=AVDD=2.5V; AVD33R=AVD33G=AVD33B=3.3V; VREFIN=1.235V; RL=37.5ohm; CL=10pF; RSET=386ohm; Temp=75oC, unless otherwise noted)

Table 4-3 AC Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Condition
CK period	Tck	5	--	--	Ns	
CK to valid output	Tdelay	--	--	0.5*Tck+2	Ns	
Output rise time	Tr	--	--	4	Ns	10% to 90% IOFS; assume no package inductance.
Output fall time	Tf	--	--	4	Ns	90% to 10% IOFS; assume no package inductance.
Output settling time	Tsettle	--	--	TBD	Ns	assume no package inductance
Glitch energy	--	--	--	--	pvs	assume no package inductance
DAC to DAC crosstalk	--	--	TBD	--	Db	.

4.4 Analog Processing and A/D Converters

Table 4-4 Analog Spec.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zi	Input impedance, analog video inputs	By design	500			k Ω
Ci	Input capacitance, analog video inputs	By design		10		pF
Vi(pp)	Input voltage range†	Ccoupling = 0.1 μ F	0		0.75	V
Δ G	Gain control range		0		12	dB
DNL	DC differential nonlinearity	A/D only		± 0.5		LSB
INL	DC integral nonlinearity	A/D only		± 1		LSB
Fr	Frequency response	6 MHz		-0.9	-3	dB
SNR	Signal-to-noise ratio	6 MHz, 1.0 Vp-p		50		dB
NS	Noise spectrum	50% flat field		50		dB
DP	Differential phase		1.5			
DG	Differential gain			0.5%		

4.5 I²C Host Interface Timing

Table 4-5 I²C Interface Timing

	Parameter	Min	Typ	Max
t1	Bus free time between a Stop and Start condition	4.7ns		
t2	Hold time (repeated) Start condition	4.0us		
t3	Rise time of both SDA and SCL			1000ns
t4	Data hold time	5.0us		
t5	Data setup time	250ns		
t6	Fall time of both SDA and SCL			300ns
t7	Setup time for a repeated Start condition	4.7us		
t8	Setup time for Stop condition	4.0us		
tLow	Low period of the SCL	4.7us		
tHigh	High period of the SCL	4.0us		
fSCL	SCL clock frequency			1Mhz
Cb	Capacitive load for each bus line			400pF

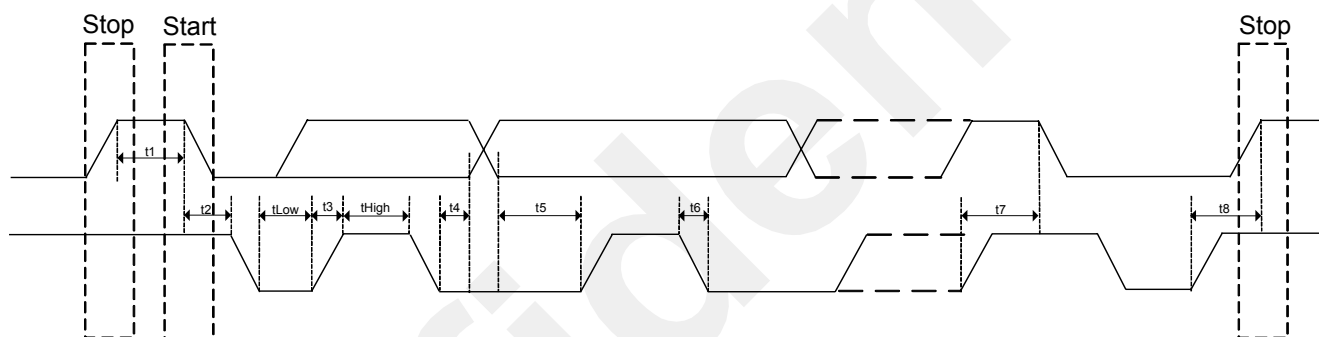


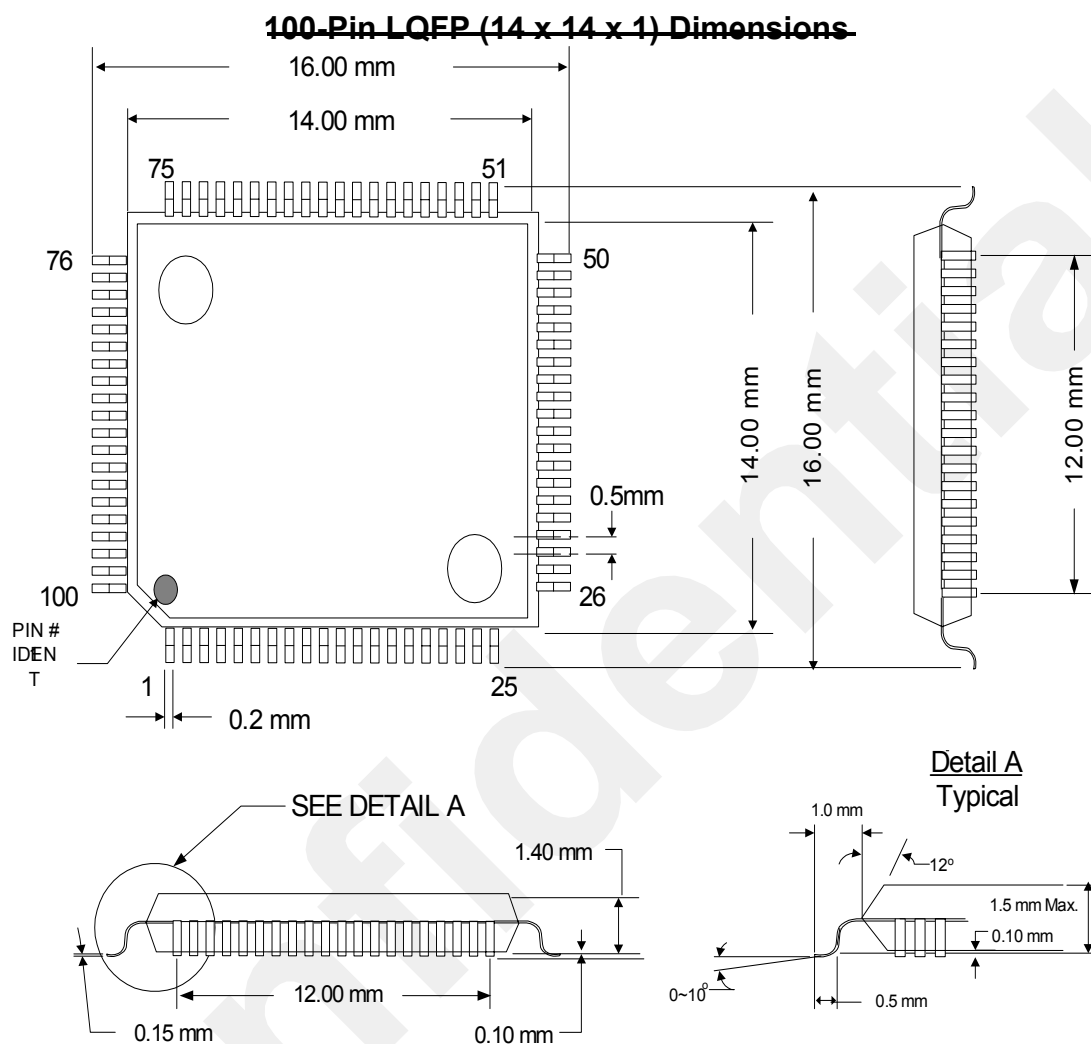
Figure 4-1 I2C Timing Waveform

4.6 Absolute Maximum Rating

Table 4-6 Maximum Rating

	Parameter	Min	Max	Unit
Topr	Operation Temperature	-20	+85	°C
Tstg	Storage Temperature	-65	+150	°C

5 Package Dimensions



[100 LQFP 14 X 14 X 1.4 mm]

Figure 5-1 Package Dimension

6 Ordering Information

Part No.	Package
T102	100 LQFP

7 Revisions Note

Table 7-1 Revision Note

Revisions	Description of changes	Date	Note
0.1	First draft	Feb 25, 2005	
0.2	Descriptions Correct	June 7, 2005	

8 General Disclaimer

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